ABSTRACT

Title of Document: EFFECT OF INTERMETALLIC GROWTH ON DURABILITY OF HIGH TEMPERATURE SOLDERS (SNAG, SAC305, SAC+MN, SNAG+CU NANO) IN THERMAL AND VIBRATION ENVIRONMENTS

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The RoHS ban of lead from electronics has pushed the industry to find lead free alternatives. In high temperature environments, high lead solders have typically been used. A suitable lead free replacement alloy is required. In this study quad flat packages (QFP) and 2512 chip resistors soldered with commercially available Sn3.5Ag and SAC305, and experimental SAC+Mn and SnAg+Cu Nano alloys on ENIG finished copper were subjected to three tests. Isothermal aging at 185°C for up to 1000 hours and at 200°C for up to 500 hours were performed to measure the interfacial intermetallic thickness, assess intermetallic compounds, and view the microstructure. A durability assessment was performed featuring thermal cycling ranges of -40 to 185°C and -40 to 200°C intermixed with 50G vibration cycling to determine the most durable solder alloy. Failure analysis was performed to understand the durability results. Finally, shear testing was performed to determine a correlation between shear strength and durability. The results show SAC305 is the most reliable solder under these conditions.

EFFECT OF INTERMETALLIC GROWTH ON DURABILITY OF HIGH TEMPERATURE SOLDERS (SNAG, SAC305, SAC+MN, SNAG+CU NANO) IN THERMAL AND VIBRATION ENVIRONMENTS

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Dedication

To my parents, Beth, Jon, and Jess.

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Chapter 1: Introduction

In modern society, electronics are widespread in nearly every aspect of life, including business, technical innovation, and entertainment. The adoption of electronics into the mainstream has been rapid. Digital cameras, smart phones, and laptops are no longer novel items but commonplace. When comparing products of similar functionality, reliability is a decisive factor for market success. Therefore, reliability growth is a core goal for all electronic packaging research.

The variety of electronics corresponds to an assortment of environments in which electronics are required to operate. Commercial electronics dominate the industry today, functioning in relatively mild conditions. Other sectors require use under far more severe working conditions. Military applications, for example, necessitate extended life cycles in a wide range of climates, including arid desert, frozen tundra, and humid jungles. Maximum operating temperature can be used to classify electronics by end use, as shown in Table 1 [1].

Table 1: Classification of Electronics Operating Environment [1]

Classification	Temperature Range (°C)
Commercial	0 to 70
Industrial	-40 to 85
Automotive	-40 to 125
Military	-55 to 125

1.1 Harsh Environments

Harsh environments are typically characterized by high operational temperature, shock or vibration, humidity, contaminants, and radiation. The automotive, space, military, and

energy industries can subject electronics to harsh environments with each end use posing its own challenges. In deep energy exploration, either for fossil fuels or geothermal fields, electronics are subjected to extreme temperature and shock or vibration loading. Ambient temperature near the electronics is in excess of 200°C with shock and vibration loading. The ambient temperature in deep energy exploration impedes the ability to thermally manage electronics thus creating a need for electronic devices with materials that can withstand such temperatures.

1.2 Surface Mount Soldering

Manufacturing printed circuit boards (PCB) requires a joining method between the chip or device and the leads on the PCB. Soldering is the standard process for joining the package leads and PCB into one continuous circuit. Thus, a solder joint must provide electrical conductivity, mechanical strength, and a thermal pathway. Through-hole soldering has been replaced by surface mount attachment due to increased interconnection density and the ability to miniaturize connections.

Surface mount soldering utilizes a reflow process and solder paste. Solder paste is a combination of the metal alloy powder mixed into a viscous flux that aids in the reflow process. Solder paste is deposited through a stencil onto the PCB leads, a device is then placed over the leads in the solder paste, and the PCB is placed in a reflow oven. The temperature is increased until the solder alloy is above liquidus for about one to two minutes and then cooled to room temperature. After cooling, a solidified solder joint has been created joining the chip lead and the PCB lead. A reflow process for SAC305 is displayed in Figure 1, acquired from the FCT Assembly SAC305 data sheet [2]. The

standard reflow process consists of four regions: preheating, flux activation, reflow, and cooling, taking only a few minutes to form solder joints.

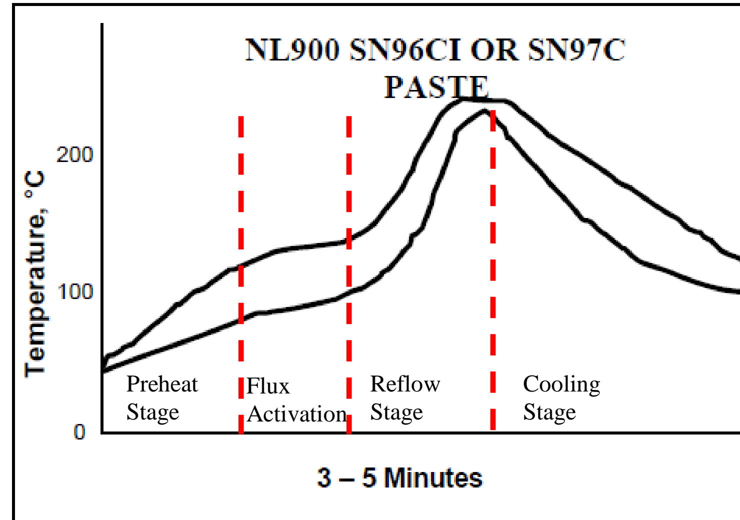


Figure 1: SAC305 recommended by FCT Assembly data sheet [2].

Solder joint creation requires intermetallic reactions at the surface of the copper pad and at the chip lead level in order to establish a strong bond, forming a thin intermetallic layer during reflow. This layer is stronger but more brittle than the bulk solder. Therefore, increasing thickness of the interfacial IMC layer is deemed detrimental to reliability under mechanical stresses. Diffusion, occurring more rapidly at higher temperatures, causes the interfacial intermetallic layers at the interface to grow more quickly as a function of time. Suppressing the growth of the intermetallic layer at the copper pad interface appears to be a promising method to increase the reliability of solders at elevated temperatures.

1.3 Identification of High Temperature Solders

Article four of RoHS directive 2002/95/EC bans the sale of electronics containing lead after July 1, 2006 in the European Union (EU) [3]. Additionally, urged by market

differentiation, many Japanese companies have self imposed regulations to remove lead from electronic systems [4]. The interdependence of the global market and international corporations has created a worldwide push to remove lead from electronics. While no formal legislation in the United States bans lead from electronics, the industry has responded to the EU ban and Japanese trends by moving toward lead free electronics.

Prior to the ban of lead on electronics in the EU, eutectic tin lead solder was the most common solder. Additionally, a wide range of lead-based solders were developed for various applications and operational environments. Lead free replacements for these solders are required. Two problems are an inherent result of conversion to lead free solders. First, the higher melting temperature of lead free solders (~220°C) risk damage to other devices during reflow, and second, cost is increased due to more precious metals being used in lead free solders than in leaded solders.

Binary lead free systems include eutectic tin-silver, tin-copper, and tin-antimony, however no system was deemed an ideal replacement of binary tin lead. Adding a third element to a binary system has held promise; tin silver copper (SAC) alloys are commonly used as solders. Low silver content SAC alloys such as SAC105 are preferred in shock and vibration environments due to longer joint life [5]. Increasing the silver content reduces the creep rate of SAC solders thereby increasing reliability when subjected to temperature aging [6]. Thus, high silver content SAC alloys such as SAC405 are selected for high temperature applications. SAC305 is generally regarded as the compromise between silver content SAC alloys and used in most applications.

1.4 Research Motivation

The research presented in this thesis is motivated by the requirement to find a lead free solder that performs reliably in both high temperature and high vibration environments. The rapid growth of interfacial intermetallic layers at extreme temperature appears to be areas of concern in solder joint reliability. The focus of this research will first identify minor additions to lead free solders that are expected to suppress the interfacial intermetallic growth. Next isothermal aging tests will be conducted to assess interfacial intermetallic growth of lead free solders containing these additions. These solders will then be subjected to reliability testing combing isothermal aging, thermal cycling, and vibration cycling. Finally, shear testing of solder joints will be performed to compare shear strength to reliability or interfacial intermetallic thickness.

Chapter 2: Literature Review

In this chapter, the results of previous work regarding high temperature solder joint reliability, motivation to suppress interfacial intermetallic layers, techniques to improve solder intermetallic formation, and the impact of various surface finishes are reviewed. The assessment of solder techniques focused on both commercially available solders as well as experimental solders. After sufficient evaluation, the experimental choices were selected and will be discussed at the end of the chapter.

2.1 High Temperature Reliability

Many applications such as aeronautic, military/space, automotive and deeper energy exploration operate at high temperature, however there is very little research assessing the reliability of lead free solders in harsh environmental temperatures. It must be noted that the RoHS legislation includes an exemption of the use of high melting temperature solder containing more than 85% lead, which are typically used in harsh environments [3]. This current exemption may explain the lack of research however it should not be used as a shield to avoid removing lead from solder in all applications.

In 2001, Gaye et al. published the results of a four year industrial consortium studying lead free solders at high temperature [7]. This study is believed to be the first study assessing lead free solders reliability at temperatures above 150°C. Using a variety of components, 20 I/O leadless ceramic chip carriers (LCCCs), 1206 chip resistors, 0805 chip resistors, 80 lead quad flat pack (QFP), and ball grid array (BGA), seven lead free solders were studied from an original list of 241 alloys, on imidazole finished copper surfaces. The data for the QFP and BGA packages were not presented due to lack of failures or early failures due to processing. The LCCCs and chip resistors both showed

that SAC405 outperformed eutectic SnAg. However, the authors concluded significant effort would be required to find a suitable replacement for high lead solders because insufficient results had been obtained.

Other studies compared lead free solders to leaded solders to assess the change in performance. Schubertt et al. utilized flip chip assemblies with aluminum pads coated with electroless nickel placed on FR-4 test boards with Cu/Ni/Au finish leads using SAC405 and Sn37Pb solder bumps cycled from -55 to 150°C [8]. The test results suggest improved fatigue life of SnPb solder joints for relatively stiff components and high thermal mismatch induced loads compared to better performance of SAC405 solder for relatively compliant structures and low thermal mismatch induced loads. Suhling et al. used 2512 chip resistors soldered with SAC387, Sn3.35Ag1Cu3.3Bi, Sn3.8Ag0.7Cu2Bi, Sn3Ag0.5Cu8In and Sn37Pb on electroless nickel immersion gold (ENIG) finished FR-4 test boards cycled from -40 to 125°C and -40 to 150°C [9]. At the higher temperature range Sn37Pb outperformed lead free solders significantly. Failure analysis showed cracks form under the component and follow the resistor leads until failure. Both of these studies confirm that at high temperature large mismatch thermal expansion strain causes failure more rapidly in lead free solders than eutectic tin lead solder.

More recently, George et al. used BGAs, QFPs and chip resistors soldered with SAC305 and SnAg on ENIG and Sn-based finish polyimide boards [10]. After 1650 thermal cycles from -40 to 185°C, no statistical difference between the performance of SAC305 and SnAg in durability was found.

In these four studies, reliability of the solder joints was assessed using electrical monitoring of a variety of component types. In general, SAC405 appears to be superior in high temperature cycling compared to other lead free alloys but performance for high strain packages is still inferior to lead alloys. Other studies have attempted to assess reliability of lead free solders at high temperature with different methods. Choi et al. studied the microstructural deformation caused by 1000 thermal cycles from -15 to 150°C in the solder bulk of Sn-3.5Ag, SAC405, Sn-2Ag-1Ni-1Cu, and Sn-2.5Ag-0.5Cu-0.5Ni reflowed on a copper substrate [11]. Cycling readily produces deformation and damage in all solders. SnAg and Sn2Ag1Cu1Ni showed the most deformation and damage, Sn2.5Ag0.5Cu0.5Ni showed the least surface degradation and SAC405 appeared to have the greatest extent of non-uniform plastic deformation and damage.

In 2010 a study by Oak Ridge National Laboratory assessed SnAg as a die attach on an ENIG plated direct bond copper (DBC) substrate subjected to 1102 thermal cycles from 5 to 200°C [12]. X-Ray transmission radiographs assessed joint quality during cycling. With subsequent cycling an increasing void fraction was viewed due to thermal fatigue, creep, and fatigue-creep interactions. Pre-existing voiding did not grow during cycling but numerous small cracks/voids developed. Numerical modeling of damage and void growth did not agree with the experimental results of Sn-3.5Ag, requiring further study potentially due limited data of Sn-3.5Ag properties at high temperature.

Finally, high temperature aging studies have used shear testing to estimate reliability. Ma et al. used thermal aging and shear strength to predict solder joint reliability [13] at elevated temperatures. SAC405, SAC305 and Sn37Pb were subjected to aging at 80, 100,

125, and 150°C for 0-6 months. Strength and creep tests were performed to estimate reliability. Preliminary results at 150°C show that both SAC305 and SAC405 see a greater reduction in strength when aged for 100 hours at 150°C than at 125°C. The strength reduction is due to microstructural coarsening of the grains. A full set of results at 150°C have not been published. Yoon et al. assessed BGA packages with Sn-0.7Cu and Sn-3Cu on ENIG finished copper FR4 test boards [14]. Aging was performed between 70 and 170°C for 1 to 100 days. Significant reduction in shear strength was seen after only one day of aging for all elevated temperatures indicating less reliable joints. However, the authors attribute this loss in strength to a copper solubility in the tin matrix rather than interfacial intermetallic growth.

Several conclusions are apparent from these high temperature studies. First, insufficient study of the reliability of lead free solder above 150°C exists. Without more data, solid conclusions are difficult to make. Additionally, the component stiffness and thermal expansion mismatch greatly impacts the reliability at high temperatures for lead free solders. Finally, no replacement solder has been found for temperatures above 150°C, thereby requiring further study.

2.2 Interfacial Intermetallic Layer

The structural integrity of a solder joint is dependent on the interfacial intermetallic reactions. To form good joints, chemical reactions that form intermetallic compounds at the solder surface interface must occur to bond the solder material with the component lead or printed circuit board. However, overgrowth of these intermetallic layers presents a reliability problem. Due to the adoption of lead free solder, the work to understand the intermetallic compounds and their effect on solder joint life must be performed. Three

factors control the intermetallic layer compounds and growth; the solder alloy, the surface finish on the component and the PWB, and the assembly process [15].

Over the past decade many studies have worked to understand the intermetallic layer compounds and growth models of various lead free solders and surface finish combination. Several consensuses amongst researchers concerning intermetallics have been reached. First, intermetallic layers grow as a function of time and grow faster at elevated temperatures [14][16][17][18][19][20][21][22][23][24]. This presents a formidable problem for high temperature applications that will rapidly accelerate intermetallic growth. Also, many researchers agree that interfacial intermetallic layers growth due to interdiffusion kinetics and according to Equation 1 [17][20][21][22][24].

$$d = d_0 + \sqrt{\mathrm{Dt}} \tag{1}$$

Where d_0 is the initial thickness, D is diffusivity, and t is time. The diffusion component can be described by an Arrhenius equation as such

$$D = D_0 \exp\left(-\frac{\mathrm{Q}}{\mathrm{kT}}\right) \tag{2}$$

where D_0 is a constant independent of temperature, Q is activation energy, k is the Boltzmann constant, and T is absolute temperature. Another consensus involves processing. Holding the peak temperature during reflow for longer durations increases the initial intermetallic layer thickness and changes the morphology [17][22]. Therefore, shorter peak temperatures are advantageous.

Finally, accelerated tests and failure analysis have shown that as the intermetallic layers grow failure locations move into the interfacial intermetallic layers

[14][17][18][19][20][22][23]. This is generally attributed to the weaker interfaces between intermetallic layers and bulk solder as well as the high modulus of elasticity of intermetallic compounds increasing the stress in those layers. Zhu et al. utilized persistent slip bands at a 45° angle that were impinged onto the solder joint, in order to determine if the intermetallic layer was more susceptible to cracking or if the intermetallic/copper substrate interface would delaminate. The study concluded the brittle intermetallic layer is subject to cracking rather than delaminating, thus a thicker layer poses as a reliability concern [25].

Other effects such as intermetallic layer roughness and the impact of substrate roughness on intermetallic growth have been studied. As intermetallics increase in thickness, the roughness also increases, which causes cleaving failures [18]. This result was studied further by Rodekohr et al. who assessed roughness of the intermetallic layers as a function of surface finish roughness [21]. This study confirmed that increasing intermetallic thickness increases the interface intermetallic layer roughness. Additionally, if the surface finish roughness is decreased, Cu_3Sn forms more rapidly without increasing overall thickness. The Cu_6Sn_5 intermetallic is more brittle than Cu_3Sn, so this result is advantageous.

Finally, many tin based lead free solders have varying silver concentrations in the alloys. Silver intermetallics, Ag_3Sn, form in the bulk solder and can migrate towards interfaces over time. Increasing the concentration of silver within the solder alloys will create larger Ag_3Sn platelets and large needles in the bulk solder which are very brittle and often initiate fractures [16]. The results of a study by Kim et al. show that less than 3.5 wt%

silver will reduce the formation of large Ag_3Sn intermetallics, and recommend a solder alloy composition with less than 3.2 wt% silver. Coupling this finding with the high temperature reliability solder recommendation of SAC405, 4 wt% silver, SAC305, 3 wt%, appears be an alloy that optimizes these competing reliability issues.

2.3 Solder Alloy Intermetallic Layer Reduction

The intermetallic layer growth is of crucial importance to high temperature applications therefore reduction in the interfacial layer was studied. Applying the knowledge of the three controlling factors, solder alloy was chosen as the primary reduction technique. A thorough study of various lead free alloy composition and additions was used to determine ideal solder alloys. The use of a fourth element dopant in a SAC based alloy and reactive nano particles were investigated for this study.

2.3.1 Trace Element Dopant

The first method studied to reduce the interfacial intermetallic growth was doping the solder with an additional element. Good results have been obtained from doping lead free solder alloys with trace amounts of rare earth elements [26][27][28][29][30]. While this approach has been successful in the past, the volatility of the rare earth metal market was posed as a threat to the use of these dopants. Nickel and cobalt are commonly used as dopants and are studied often. Effects of cobalt and nickel tend to be very similar, resulting in a thick initial intermetallic layer after reflow which acts as a diffusion barrier and retards subsequent growth of the intermetallic layer [31][32][33][34][35][36][37][38]. Additionally, nickel and cobalt have been mixed together as a two dopant method. This approach suppresses growth but nonetheless forms a thick layer which was deemed as a reliability threat. The use of antimony as a dopant has also

shown to reduce the intermetallic layer growth as well but toxicity issues of the dopant discouraged further study [27][39][40]. Manganese as a trace element dopant has also shown positive results in intermetallic layer reduction [41]. Recent studies have used 0.05%wt Mn doped into SAC105, a low silver content solder, which is preferable in shock environment but not tested at high temperatures [42]. Higher silver content solders are typically used for high temperature applications, thus a high silver content SAC alloy with manganese dopant would be more desirable. Zinc is another element that has been discussed as a dopant. Small additions of zinc have showed positive results at limiting the voiding in copper pads after consumption into the intermetallic layer [43]. However, large additions of zinc lower the melting point of the solder below 200°C [44]. A wide variety of other elements were investigated including aluminum, iron, magnesium, indium and phosphorus. The results for these dopant elements did not show intermetallic layer suppression [32][42][43][45][46].

2.3.2 Reactive Nano Particles Additions

Researchers have suggested mixing nano sized particles into the solder bulk matrix without alloying the addition. The nano particles are expected to pin the grain boundaries in the solder bulk and slow interdiffusion kinetics thus suppressing the interfacial intermetallic formation. Additionally, grain refinement of the solder bulk is expected during aging [47]. Without alloying the nano particles both reactive and non reactive particles can be considered. A wide variety of reactive nano particles were explored including pure copper and silver, copper and silver intermetallics, and various metallic oxides. All the reactive nano particles showed positive results limiting the interfacial intermetallic layer due to the mechanisms listed previously [48][49][50][51][52][53].

Copper based nano particles are less expensive than silver nano particles, thus economics should be considered in addition to performance.

2.4 Surface Finish

In addition to solder alloy, surface finish is important to the development of interfacial intermetallics. Surface finish refers to the copper pad finish on the printed circuit board as shown in Figure 2. This layer is used to protect the copper pad from oxidation which decreases solderability. The component terminations also have a finish, typically matte tin for lead free compliant components, which is labeled termination finish in Figure 2.

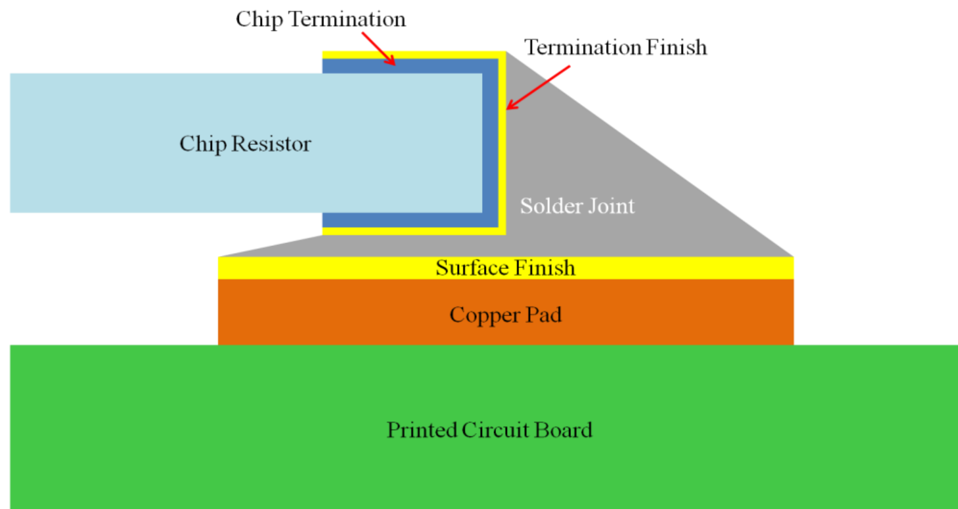


Figure 2: Example chip resistor solder joint showing surface finish.

This portion of the literature review will focus on surface finish only. The various lead free surface finish options will be discussed first, followed by a comparison of intermetallic layer growth on those finishes.

2.4.1 Review of Lead Free Surface Finishes

Many lead free surface finishes are currently available. Currently available options include, organic solderability preservative (OSP), immersion tin (ImSn), immersion silver

(ImAg), lead free hot air solder leveling (HASL), electroless nickel immersion gold (ENIG), and electroless nickel electroless palladium immersion gold (ENEPIG) [54]. The finish affects the solder joint reliability, intermetallic compounds, and cost. According to Triangle Circuits each finish has advantages and disadvantages. OSP is very cheap and prevents copper oxidation but has a poor shelf life and degrades with high temperature. ImSn provides good wettability of solder joints but is a risk for tin whiskers. ImAg has a long shelf life and low cost however ImAg must be avoided in a sulfur-rich environment. HASL provides excellent shelf life, low cost and good adhesion at the expense of poor coplanarity and process control. ENIG has excellent wettability, coplanarity, shelf-life and adhesion but ENIG has higher cost than the previously mentioned finishes and suffers from black pad [55]. Triangle Circuits does not have ENEPIG available as a surface finish. According to ROHM ENEPIG offers improved performance to ENIG without black pad but ENEPIG is more expensive [56].

2.4.2 Comparison of Finish Results

ENIG and ENEPIG finishes have shown to suppress the interfacial intermetallic layer growth better than OSP, ImSn, ImAg, or HASL [57][58][59][60]. The nickel layer in ENIG and ENEPIG serve as a diffusion barrier from the copper pad that forms interfacial intermetallic layers. ENEPIG tends to outperform ENIG due to an additional palladium diffusion barrier, which increases finish cost [59]. Choubey et al. recommends OSP for short term reliability applications due to the lowest cost and comparable intermetallic layer thickness results to ImAg and ImSn [60]. ImSn forms an initial intermetallic layer prior to reflow of the solder joint as reported by Zheng et al, which can create thicker but slower growing intermetallic layers [57]. Additionally, ImAg forms more Ag_3Sn

intermetallic particles in the solder bulk which can develop into a solder reliability issue [57][58][60].

2.5 Experimental Selections

After careful review of the literature regarding high temperature solder reliability, interfacial intermetallic layer reliability concerns, potential solder alloys and surface finishes that suppress the intermetallic layer, experimental decisions were made for this study. Four solders were selected. Two commercially available solders were chosen. Sn-3.5Ag was chosen as the baseline solder since this is the most studied lead free solder alloy. SAC305 was chosen due to the increased performance of high silver content SAC alloys during high temperature cycling without exceeding the recommended silver content to avoid large, detrimental Ag_3Sn platelets and needles. A SAC alloy, Sn-2.6Ag-0.8Cu, doped with manganese, 0.05 wt.%, was also chosen since positive results have been shown using manganese to suppress the interfacial intermetallic growth. Finally, an alloy of SnAg with the addition of pure copper nano particles was chosen due to positive results by adding nano particles into the solder matrix and availability of copper nano particles. All four alloys will be tested on polyimide test boards to withstand high temperature with ENIG surface finish. ENIG is a very popular surface finish, the nickel layer serves as a diffusion barrier to retard interfacial intermetallic layer growth, and ENIG is cheaper than ENEPIG.

Chapter 3: Solder Preparation and Test Materials Procurement

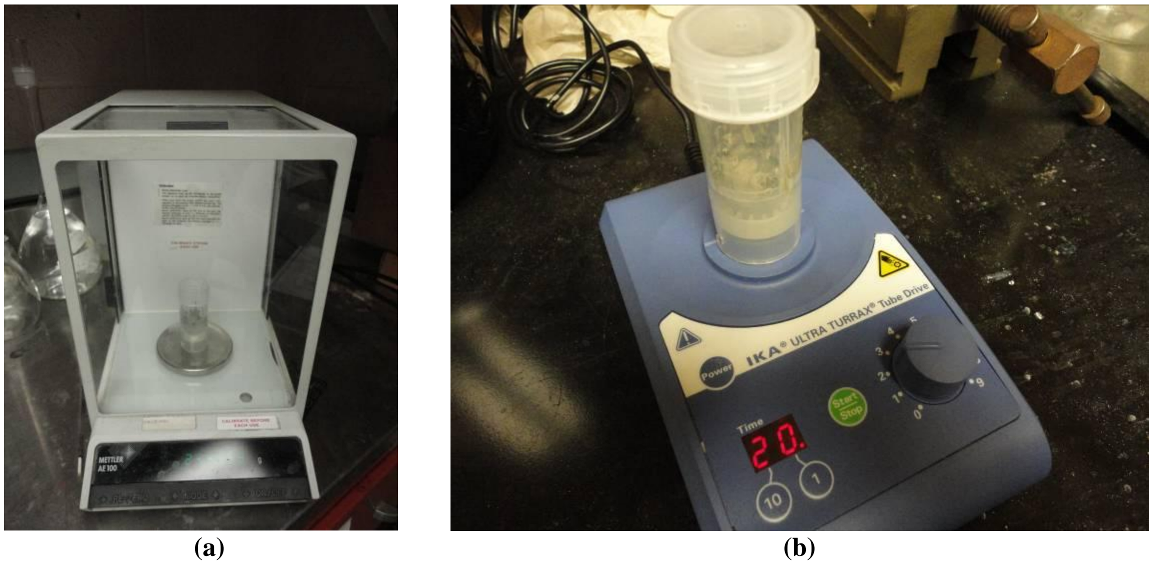
3.1 Solder Preparation

Four solders were selected for comparison in this research. Two commercially available solder pastes were used. Alpha Metals owned by Cookson Electronics manufactured the eutectic tin silver, 96.5 wt% tin and 3.5wt% silver, (SnAg) paste which was obtained through Hisco. The SnAg metal alloy powder was mixed with RMA–390 flux. The other commercially available solder selected, 96.5% tin 3.0% silver 0.5% copper, by weight, (SAC305) was manufactured by FCT Assembly and obtained through Stencils Unlimited. The SAC305 paste used a no clean flux, NL-900, to mix with the metal alloy powder.

The novel solders feature two different methods of interfacial intermetallic layer suppression. The first technique uses an additional trace element dopant into a tin-silver-copper alloy. A commercially available low silver content, 1% by weight, SAC alloy with a Mn dopant is on the market however, the goal to find a high temperature and high vibration solder made this choice less desirable. Indium Corp. supplied an experimental manganese element dopant SAC alloy (SAC+Mn) that features 2.6% silver and 0.8% copper by weight plus a trace amount of manganese, about 0.05% by weight. By increasing the silver content by about 2.5 fold, it was believed this solder would be more durable when subjected to high temperature aging and cycling. The experimental SAC+Mn solder is mixed with a no clean flux, Indium8.9E.

The final solder for this study utilized a reactive nano particle dopant. An addition of 0.5% by weight pure copper nano particles were mixed into the eutectic tin silver solder paste obtained from Alpha Metals. This solder was manufactured at the University of Maryland. The copper nano particles were obtained from Alfa Aesar as 99.9% pure

copper particles sized 20-40 nm packed under argon. Mechanical mixing is a proven, effective, and simple method to mix nano particle powder into a base solder paste [47]. A Mettler AE100 scale with precision to 0.0001g was used to accurately measure the correct weight percent of the base solder and copper nano powder dopant. The powder and solder paste were then mixed for 30 minutes at 200 rpm using an IKA Tube Mixer. Figure 3 displays the scale and mixer used to add the copper nano particles to the SnAg solder paste. A total of 400 grams of solder paste was manufactured to ensure enough solder paste was available for the stenciling process.



(a) **(b)**

Figure 3: Equipment used to create solder paste, (a) Mettler AE100 scale, (b) IKA tube mixer during use with 20 minutes remaining.

Upon arrival, or after manufacture, all solders were stored according to the data sheet recommendations, at temperatures below 10°C in a refrigerator. The solders were shipped to Schlumberger for test board assembly packed under dry ice to prevent oxidation prior to test board manufacture.

3.2 Component Selection

Two package types were selected for the study, a quad flat pack (QFP) and a chip resistor. A high input/output QFP with 256 leads was selected as the first component, supplied by Practical Components and manufactured by Amkor. The QFP features copper leads plated in matte tin which provides copper to the joint interfaces to form copper intermetallic layers. The QFP leads were daisy chained to form a continuous circuit after reflow with the corresponding board leads. The gullwing structure of a QFP lead minimizes the thermal expansion mismatch strain on the solder joint by utilizing its shape to carry deformation that would otherwise be carried by the solder joint.

The second component selected was a 0 ohm 2512 chip resistor with nickel leads plated in matte tin, also supplied by Practical Components. The chip resistor leads provide sufficient nickel to the solder joint creating a higher abundance of nickel intermetallics at the interface. Additionally, due to the size of the chip resistor and the alumina, Al_2O_3, substrate, larger thermal expansion mismatch strain is carried by the solder joint. The solder joints for the 2512 chip resistors were expected to fail more rapidly allowing for differentiation between the solders studied.

3.3 Test Board Design

To withstand the high temperature aging and thermal cycling maximum temperatures used in this experiment, polyimide test boards were selected due to a higher glass transition temperature (>400°C) than conventional FR-4 (>120°C). Solder pad finish was also selected to help suppress interfacial intermetallic layer growth. As a result of the literature study, ENIG was selected due to improved performance at an acceptable increase in cost.

The test board layout consists of two halves with the same component distribution as shown in Figure 4. A total of eight daisy chained QFPs and 24 chip resistors are placed on each test board. The 24 chip resistors are chained into eight sets of three chip resistors. The purple outline represents ¼'' thick aluminum framing attached together on both sides of the test boards by 19 bolts. The test boards will be subjected to intense loading conditions that are representative of field conditions. Harsh environment electronics typically include systems to increase durability. The aluminum framing was used to simulate harsh environment electronics additional design considerations.

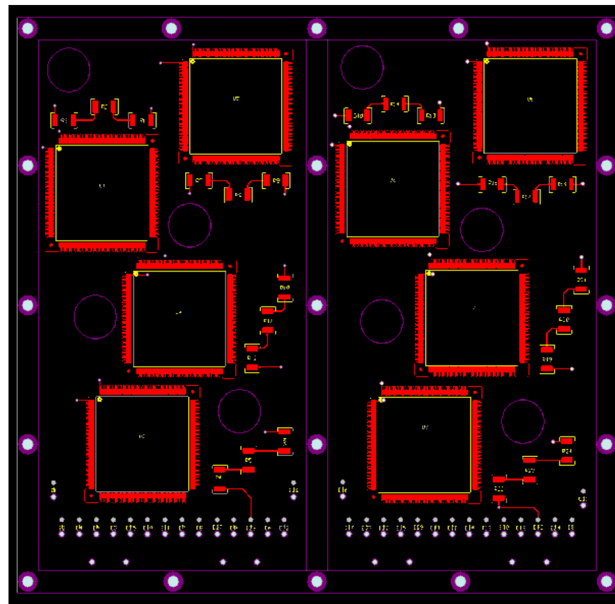


Figure 4: Test Board Layout

The test boards were fabricated and processed by Schlumberger utilizing the four different solders. One solder was used per board for ease of manufacture. Two different reflow profiles were used for the four solders. SnAg and the SnAg+Cu Nano both utilized the Alpha Metals optimized reflow profile. The addition of pure copper nano particles are not intended to change the alloy chemistry and were therefore not expected to impact the solder joint reflow process. The SAC305 and SAC+Mn used the recommended SAC305

reflow profile. SAC+Mn does not have an optimized reflow profile since it is an experimental solder. Due to the similarity in composition to SAC305, this profile was used for the SAC+Mn solder.

The boards feature resistance monitoring for the components utilizing a strain relieving wiring system. High temperature Teflon coated Weico wire no. 2324, rated to operate reliably in the range from -60°C to 200°C, was used as the monitoring wire. The monitoring wires were soldered using SAC0305 wire solder to an ENIG plate through-hole. The wire was inserted through a drilled hole at the bottom of the board and bent back and inserted through the ENIG plated through-hole, leaving a loop between the monitoring joint and backside of the board. All the wires from each half of the board were clamped by the board framing to minimize wire movement and strain that can cause monitoring wire failures.

3.4 Test Equipment

The experiment features both isothermal aging and thermal cycling. A Blue M Electric convection oven was used for thermal aging and a Sun Electronic Systems EC-12 convection chamber was used for thermal cycling. The Blue M Electric convection oven maintains stable temperatures over 300°C, well within the temperatures desired for this experiment. The EC-12 chamber has the capability to cool as low as -184°C utilizing liquid nitrogen and to heat up to 315°C, with ramp rates up to 15°C/min [61].

Minimally evasive racks were built for both chambers to allow for multiple boards to be aged or cycled at once. Both chambers use forced convection for heating/cooling; therefore racks were built that minimize the obstruction to air flow. Galvanized steel wire

mesh cloth and ¼'' all-thread was used to create multi-level racks that have minimal cross section in the direction of air flow. Figure 5 shows an example of one rack with the direction of airflow into the page when the rack is placed in the chamber.

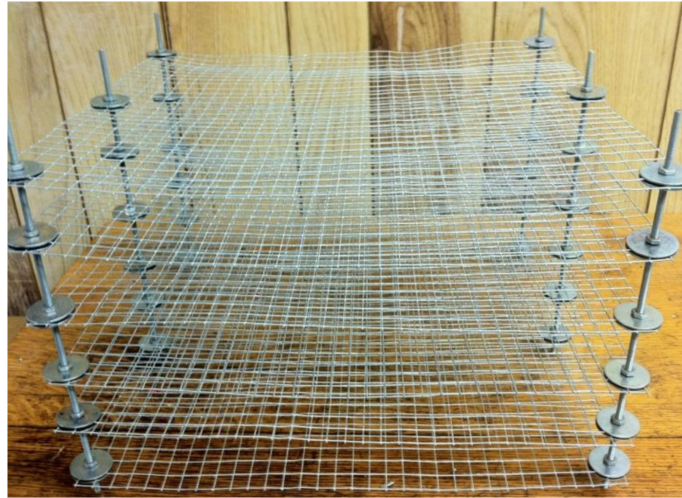


Figure 5: One of two test racks built.

A Data Physics Signal Force uniaxial shaker was used for vibration cycling. This system allows a sinusoidal input force to be imparted onto a fixture at a prescribed frequency. The control software displays the G force on the test boards that is measured by the control accelerometers. This system allows for tuning to set the correct frequency that outputs the desired G force on the test boards. The Signal Force fixture clamped the ends of the test boards in an aluminum fixture that amplifies the imparted force. This fixture design allows for high G vibration on the test boards. An "add-on" fixture was built to support the test boards in the x and y axes using aluminum L's to clamp the test boards.

A Dage2400 shear tester was used to shear the 2512 chip resistors. The Dage2400 utilizes a die shear cartridge that is capable of applying up to 20 kilograms of force at a rate up to 36mm/minute. The clamping fixture is attached to the Dage2400 by a vacuum system that allows for movement prior to testing. Fine controls allow for alignment

between the chip resistors and shear cartridge blade. In Figure 6, the Dage 3400 with the shear cartridge is shown along with the clamping fixture.

Figure 6: Dage 2400 with shear cartridge.

Initializing the test lowers the shear blade until it makes contact with the test board, then the blade raises to the shear height and begins shearing.

3.5 Monitoring Systems

Thermal monitoring was performed by Omega K-type and T-type thermocouples, calibrated for use in an Agilent 34970A with a 20-Channel input card data logger. The accompanying software, Benchlink 3, was programmed to record the temperature every 30 seconds during thermal cycling. The output data was used to compare time to failure in minutes in terms thermal cycles.

In-situ electrical monitoring of resistance during thermal and vibration cycling was utilized to determine solder joint failures for the daisy chained QFPs and chip resistors. An ANATech STD 256 was used to measure the resistance. The ANATech software,

WinDatalog, has a built in feature to determine time to failure according to IPC-SM-785 failure criteria. Any time the resistance of a channel, either daisy chained QFP or chip resistor chain, is in excess of 300 ohms an event is registered. The IPC-SM-785 failure criteria is met when ten events occur within a number of cycles that is 10% of the cycle number of the first failure for the channel [62]. For example if the first failure occurs in cycle 200, nine more failures must occur in the next 20 cycles to determine a failure. For thermal cycling, cycles were set to 10 minutes with a poll period of 30 seconds, which results in a total of 20 measurements per cycle. The failure data was then super imposed over the thermal cycling data to determine the number of thermal cycles to failure. For thermal cycling, due to the high rate of vibration cycling, the ANATech measurement cycles were 32 seconds with a 2 second poll period, thus 16 measurements per cycle. Failures could not be correlated to vibration cycle because the vibration frequency was over 500 Hz which would require a poll rate of at least 5000 Hz which is beyond the capability of the ANATech.

The output G force on each test board was monitored at four locations during vibration cycling in the z-axis and at one location in the x and y axes. Utilizing the software scheduler, two accelerometers were moved during planned pauses in vibration cycling to allow measurement at all four locations with the same frequency and amplitude.

Chapter 4: Design of Experiment

In this chapter the details of the experimental design and procedures will be discussed. Based on the motivation to develop a durable high temperature and high vibration solder three tests were developed to assess the four selected solder choices. The first test is an isothermal aging test at maximum temperature above 150°. This test will assess the intermetallic layer growth at the interface between the bulk solder and the ENIG plated copper pads. The next test will utilize the thermal cycling and vibration cycling in order to assess the reliability of the solders. Additionally, intermetallic layer thickness will be measured at the conclusion of testing to determine the effect of thermal cycling and mechanical stressing on the growth of intermetallic layers at the interface. Finally, shear testing will be performed to develop a potential correlation between shear strength and reliability or interfacial intermetallic layer thickness.

4.1 Aging Test

After reflow an initial intermetallic layer is formed at the copper pad interface. Diffusivity is a temperature dependent parameter that increases as a function of temperature. At high temperature the increased diffusivity allows for rapid formation of interfacial intermetallic layers.

Isothermal aging was used to determine the growth of interfacial intermetallics of the four test solders. 185°C and 200°C were chosen as isothermal aging temperatures that are representative of harsh environment these solders are desired to operate. A baseline condition after reflow was used for both aging temperature tests. The other three aging times are displayed in Table 2.

Table 2: Isothermal aging time for each temperature

185°C Aging Times	200°C Aging Times
0 hr	0 hr
100 hr	100 hr
300 hr	300 hr
1000 hr	500 hr

4.1.1 Homologous Temperature Calculations

The melting temperature of SnAg is 221°C and SAC alloys melting temperatures range from 217°C to ~220°C since they are not eutectic alloys [63][64]. The homologous temperature was calculated for SnAg and SAC305. The homologous temperature is defined as the percentage of the melting temperature that a material temperature is subjected to in the absolute temperature scale, as described by Equation 3.

$$T_H = \frac{T}{T_{mp}} = \%T_{mp} \tag{3}$$

Using Equation 2, SnAg has a homologues temperature of $T_H = 0.927T_{mp}$ when aged at 185°C and $T_H = 0.957T_{mp}$ when aged at 200°C. The SAC305 calculation used a melting temperature of 217°C which is the temperature at onset of melting. SAC305 has a homologues temperature of $T_H = 0.935T_{mp}$ when aged at 185°C and $T_H = 0.965T_{mp}$ when aged at 200°C.

4.1.2 Aging Chamber Characterization

Isothermal aging was performed using a Blue M Electric convection oven. Prior to aging, a 24 hour chamber assessment was performed at 185°C. The results of the isothermal characterization are show in Figure 7. IPC Standard 9701A establishes guidelines for isothermal aging. The temperature must stay within the range of (0, +5°C) of the selected aging temperature [65]. The 24 hour assessment proves the Blue M Electric oven maintains this standard. The aging temperature is always within the 185-190°C range

except for measurement points when it is slightly below 185°C, less than 0.2°C below. This deviation is within the error range of the thermocouples and can be ignored as a potential problem. Test boards were aged on the minimally evasive wire rack so multiple boards could be aged at once.

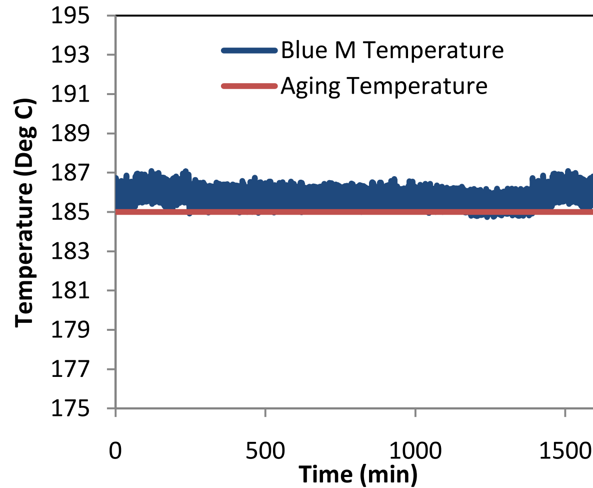


Figure 7: Blue M Chamber Characterization

4.1.3 Cross Sectioning Parameters

In order to characterize the interfacial intermetallic layers, after steady state aging, a QFP was cross sectioned and interfacial intermetallic layer thickness measurements were taken for the 185°C test. For the 200°C test a QFP and chip resistor were cross sectioned and intermetallic layer thickness measurements were taken.

All cross sections were cold mounted in 1 ¼” diameter epoxy cylinders in order to use a Buehler AutoMet 250 automatic polisher. Grinding and polishing was performed using Buehler recommendations for electronic sample preparation with copper, nickel, and soft solder present. First, using 600 grit silicon carbide grinding papers, samples were ground to the leading edge of a gull-wing QFP or the leading edge of a chip resistor. At this stage each sample was ground individually to account for the differences in potting. The

Automet 250 can polish up to six samples after all samples are brought to the same plane using individual pistons to apply pressure to each sample. The samples were then polished using 3 µm diamond abrasive in wax with a lubricant to prevent sample heating. Ultrasonic cleaning for 2 minutes was performed to remove any diamond abrasive on the sample surface. Next, the samples were fine polished using a 0.05 µm alumina suspension. The final polishing was done for each sample individually rather than in a batch process. Finally, the samples were ultrasonically cleaned for 3 minutes to remove the alumina suspension on the cross section surface. The default procedure is outlined in Table 3. At each stage samples are checked using an optical microscope at magnification of 500x to ensure scratches are removed from the previous step. The samples were cleaned with ethanol and dried with air to slow oxidation. Additional polishing was performed as necessary. After polishing the samples were etched using 94% ethanol, 4% nitric acid and 2% hydrochloric acid for 4 seconds.

Table 3: Polishing Protocol

Abrasive	Load (lbs)	Time	Base Speed	Base Direction
600 Grit SiC Paper	5	Until Plane	240 rpm	CW
3 µm Diamond Paste	4	3-5 min	150 rpm	CCW
Ultrasonic Cleaning		2 min		
0.05 µm Alumina Suspension	4	2-3 min	150 rpm	CCW
Ultrasonic Cleaning		3 min		

4.1.4 IMC Thickness Measurement Method

Once the cross sections were prepared, an environmental scanning electron microscope (ESEM) was used to view the intermetallic layer thickness. Imaging software connected to the ESEM, XTDocument, was used to determine the total area of the interfacial intermetallic layer and divided by the horizontal distance to obtain an average thickness

for each image. Each sample was viewed at 2500x magnification with three images of the intermetallic layer for QFPs and four images of the two chip resistor joints to ensure accurate results across the solder pad as the thickness deviates. Figure 8 shows the methodology used to measure the average intermetallic thickness for each image. The results for each image were averaged to obtain the sample average intermetallic layer thickness.

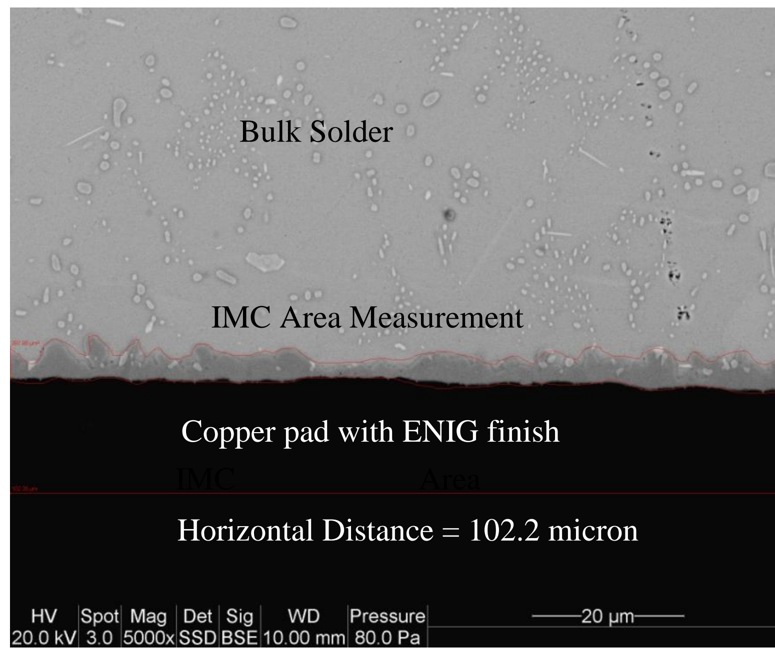


Figure 8: Sn-Ag 0hr aging, 2512 chip capacitor, interfacial IMC thickness measurement (courtesy CALCE).

Additionally, energy dispersive X-ray spectroscopy (EDS) analysis of the intermetallic layers was used to determine the intermetallic compound composition. A comparison of the stoichiometric composition of known intermetallics was compared to the atom percentage of the elements in the intermetallic to determine the compounds. The results were then compared to previous studies to validate the results. High contrast images display intermetallic layers at the copper pad interface and in the bulk much better at the expense of a lack of differentiation between copper and nickel. For the measurements

prescribed in this test, viewing intermetallics was much more important than the assessing the copper pad finish.

4.2 Reliability Test

This experiment utilizes steady state aging, thermal cycling and vibration cycling. The aging study temperatures, 185°C and 200°C, were used as the steady state aging temperature and the maximum temperature dwell during thermal cycling. Two tests were performed based on the aging/maximum cycling temperature. Identical aging conditions were used for the reliability test to compare with the aging test. In this test, the zero point was considered after isothermal aging.

After aging, the test one trials were subjected to 200 thermal cycles with a range from -40°C to 185°C and the test two trials were subjected to 200 thermal cycles with a range from -40°C to 200°C. Both thermal cycle conditions used 5°C/min ramp rates, 15 minute dwell at the maximum temperature, and 5 minute dwell at the minimum temperature. Test one trials, -40°C to 185°C, require 108 minutes per cycle with an average temperature of 84.26°C. Test two trials, -40°C to 200°C, require 114 minutes per trial, with an average temperature of 91.93°C. The ideal thermal cycle profiles are shown below in Figure 9.

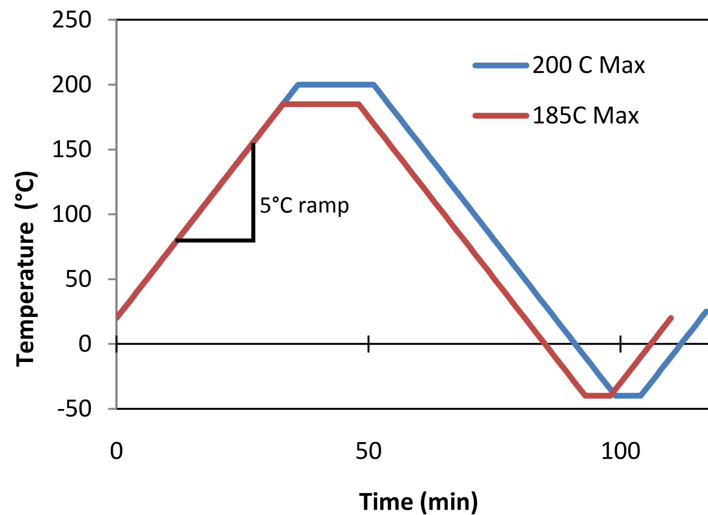


Figure 9: Ideal Thermal Cycle Profiles

Vibration cycling was intermixed with thermal cycling at intervals of 50 thermal cycles, thus the trial test boards were vibration cycled four times during testing. A total of one million 50G vibration cycles in each axis were applied as a representation of the environmental loading in harsh environments. At each interval 250,000 cycles were imparted on the test boards in each axis.

4.2.1 Thermal Cycling Chamber Characterization

Thermal Cycling was performed using a Sun Electronics EC-12 thermal chamber. Characterization of the thermal cycling chamber was required to match the measured thermal cycle with the ideal thermal cycles outlined previously. According to JEDEC standard JESD22-A104-A, the high temperature must be within the range of (0, +10°C) and the low temperature must be in the range of (-10°C, 0) in order to meet the cycle specifications [66].

- Various programming parameters were tested to find the ideal profile. In addition monitoring a single thermal cycle, the best options were subjected to a five cycle ensure the cycles were repeatable. Five thermocouples were placed in the various locations to determine temperature gradients. The program settings can be in First interfacial intermetallic compound and thickness assessment of manganese doped SAC alloy aged at 185°C and 200°C.
- First interfacial intermetallic compound and thickness assessment of copper nano particle in SnAg solder aged at 185°C and 200°C.
- First reliability comparison of the solders in this study under both thermal and mechanical stressing at temperatures above 185°C.

Appendix A: EC-12 Sun Electronics Chamber Programs. Figure 10 displays the -40 to 185 °C ideal and chamber profiles for both a single cycle and five cycles. The EC-12 thermal cycle meets the JEDEC standard. Continuous monitoring of the thermal cycles during testing was performed utilizing five thermocouples.

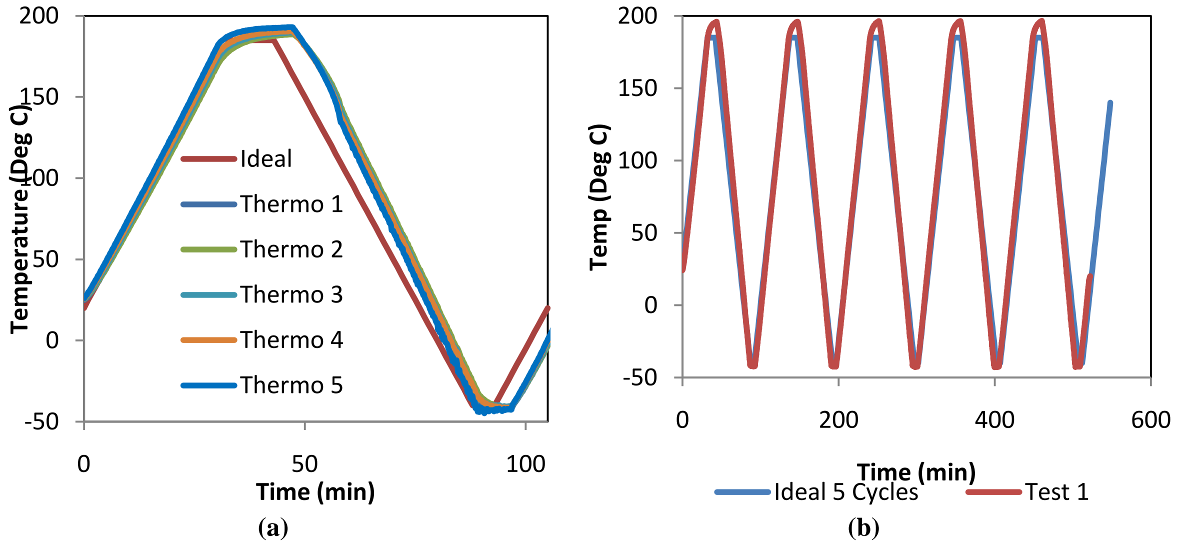


Figure 10: (a) Single thermal cycle -40 to 185 °C with five thermocouples tracking chamber gradient, (b) Five thermal cycles, -40 to 185 °C, to ensure repeatable cycles using centered thermocouple.

A similar analysis was performed for the -40 to 200°C profile. In Figure 11, the single cycle and five cycle results are shown. The profile meets the JEDEC standards for temperature cycling and was used for testing. Continuous monitoring during testing was performed to track the cycles and detect any errors in thermal cycling.

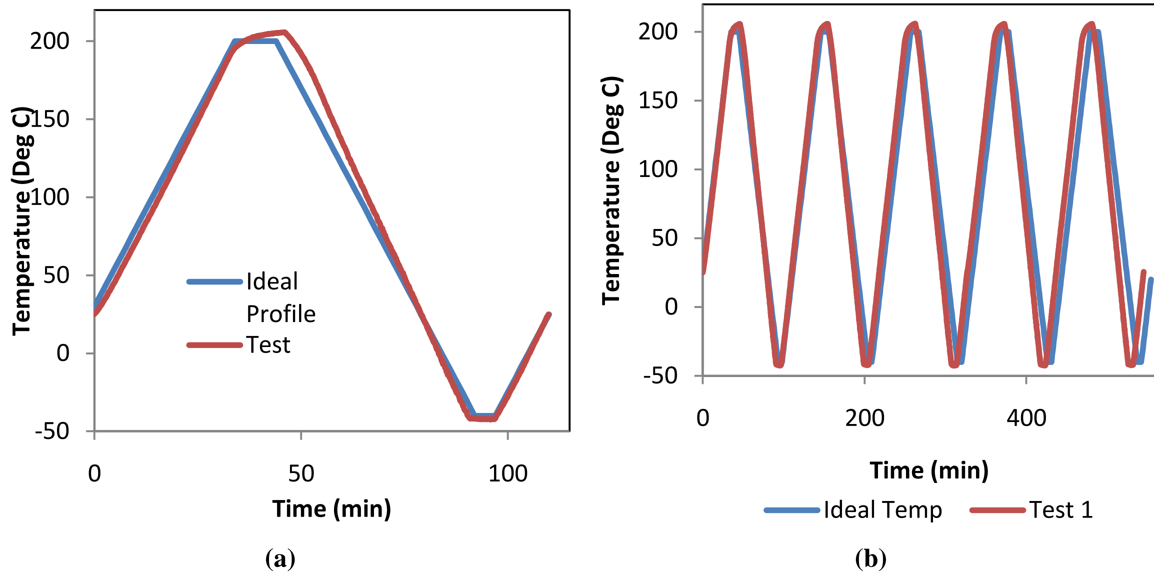


Figure 11: (a) Single thermal cycle -40 to 200 °C, (b) Five thermal cycles, -40 to 200 °C

Thermal cycling consumed considerable liquid nitrogen. During the characterization phase, liquid nitrogen dewers were tested until liquid depletion to determine operational hours. The -40 to 185°C thermal cycles consumed one liquid nitrogen dewer approximately every 32 hours requiring three dewers to complete 50 cycles. The -40 to 200 °C thermal cycles consumed a liquid nitrogen dewer approximately every 28 hours, requiring about three and a half dewers per 50 cycles. During thermal cycling, monitoring was performed multiple times a day to avoid interruptions in cycling.

4.2.2 Board / Frame Modifications

The uniaxial shaker fixture used for harmonic vibration, was only large enough to hold one complete board. Half of the board was subject to component removal during testing, which would dramatically change the board response. It was determined this problem should be assessed. By cutting the frames and test boards in half, two boards could be vibrated at once, thus halving the testing speed, and avoid an unpredicted vibration shape

on the other half. The reliability study half would be subjected to the vibration cycling and the other half, the testing components, would only be subjected to thermal cycling.

The test boards were cut using a precision Buehler IsoMet1000 diamond tipped circular saw using a blade speed of 250 rpm to minimize vibration and damage to the solder joints. The board frames were cut using an aluminum band saw. The half boards and frames were then bolted together for testing.

After cutting the boards in half, no centerline of symmetry exists, thus the vibration cycling layout must be mirrored in order to input the same vibration profile on each board. As shown Figure 12, two test boards are vibrated at once with a mirrored set up.

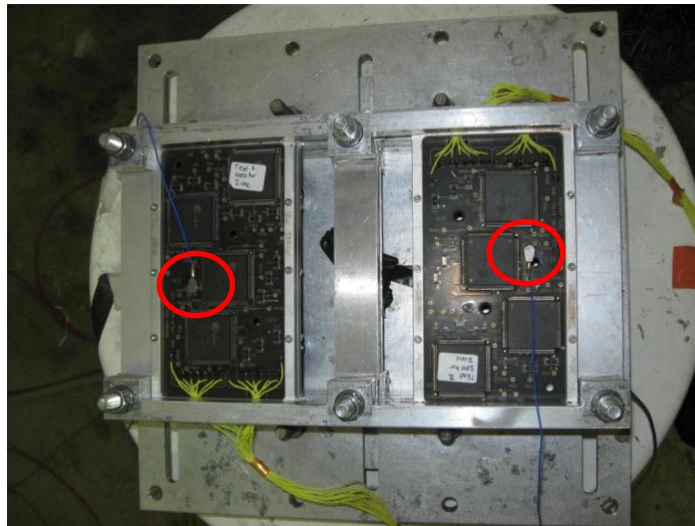


Figure 12: Uniaxial Shaker with Boards mounted

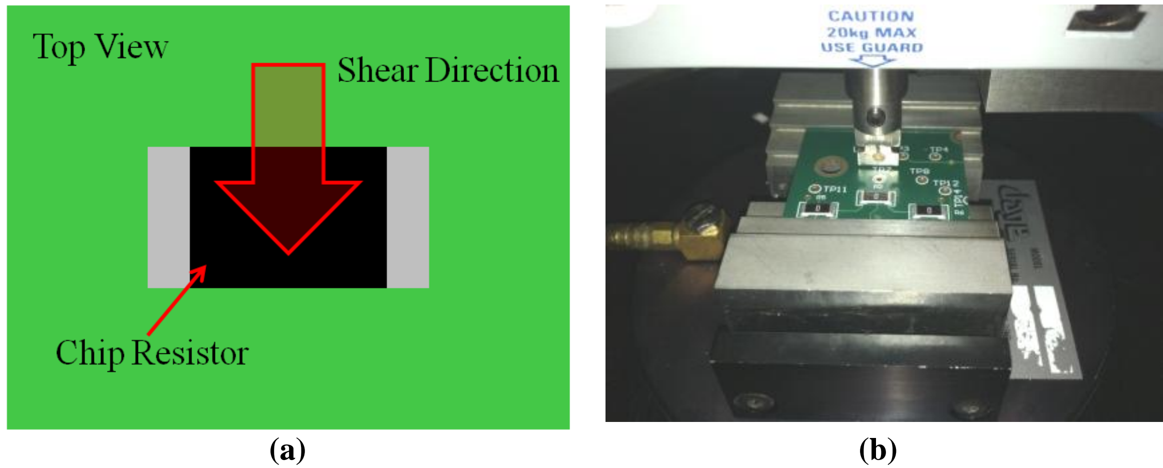
During testing, the test boards G force was monitored by accelerometers integrated into the uniaxial shaker control software. In order to assess four locations, the run schedule featured pauses to allow the accelerometers to be moved and resumed. The maximum G force accelerometer location, featured in Figure 12 by the red circles, was used to set the

initial G force of 50G +/- 1G. Every set of boards behaved differently therefore a set frequency was not used but each set of boards were tuned to 50G at the maximum acceleration location. Only one accelerometer location was used to tune the vibration to 50G in the x and y axes.

4.3 Shear Strength Test

Previous shear testing experiments were ineffective because the shear tester cracked the chip and not the solder joint, which does not represent the solder yield shear strength. This testing method was modified to improve the results. According to Choi et al, the best shear results occur when the following parameters are specified for surface mount solder joints [67]. For surface mount resistors, the best results occur when the shear rate is set to 20-40 mm/min and the lift off height is greater than 10 μm but less than 25% of the total assembly height, including solder pad.

The Dage 2400 has a 1cm wide blade that must be used for testing. The shear height was set to 50 μm and the shear rate set at 36 mm/min, the maximum shear rate of the Dage 2400. The shear direction is shown in Figure 13a as a top view along with the shear specimen clamp. The shear specimen clamp allows for test boards ranging in size from 6.5mm to 50mm in length. A screw is tightened to hold the test board specimen tightly in place. A spacer board was placed beneath the test board to ensure the clamp did not interfere with the shear chip resistor path. The fixture can be moved and adjusted to ensure the proper alignment between the shear blade and chip resistor.



(a) **(b)**

Figure 13: Shear set up, (a) shear direction diagram, (b) shear specimen in holder.

Six SnAg chip resistors were tested to ensure the parameters sheared the solder joint and did not crack the chip resistors. None of the chip resistors cracked. Optical microscope imaging revealed that the shearing had occurred at the solder joint/component lead level. Shear testing results were averaged to create a testing interval yield strength value. Additionally, after shearing the samples were viewed under the ESEM to view the fractography of the destructive testing in order to determine if the break occurred in the solder bulk or at the interface intermetallic layer.

Chapter 5: Aging Test Interfacial Intermetallic Layer Results

The first test employed to analyze the impact of the solder alloy selection was an isothermal aging test that measured the interfacial intermetallic layer thickness, assessed the evolution of the intermetallic layers, and observed the bulk structure. 185°C and 200°C were chosen as the high temperature aging conditions. This work was performed to predict the durability of the solder joints subjected to the reliability testing in the subsequent testing.

5.1 185°C Aging Results QFP Samples

The 185°C isothermal aging condition aged samples for 0, 100, 300, and 1000 hours. QFPs were removed from the test boards and cross sectioned for intermetallic layer compound determination and thickness measurements. The results of the thickness measurements for each solder and aging time are summarized in Figure 14.

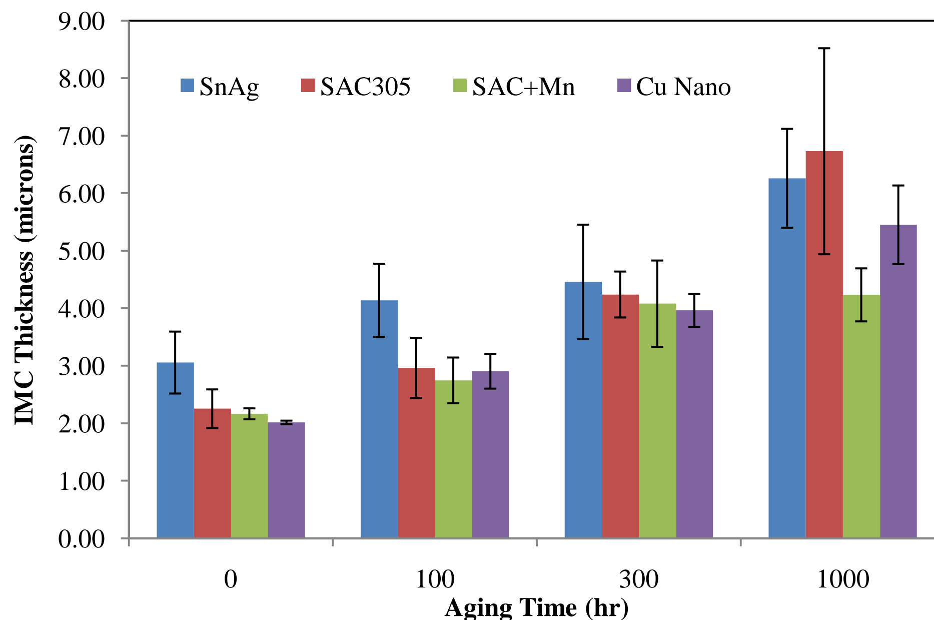


Figure 14: QFP interfacial intermetallic layer thickness results aged at 185°C up to 1000 hours.

It can be seen that the manganese dopant has a significant effect suppressing the interfacial intermetallic layer growth. The SAC+Mn thickness is almost level, non-growing, between 300 and 1000 hours indicating the layer has stabilized. The impact of the copper nano particles also mitigates the interfacial intermetallic growth. However, after long aging it is less effective than the manganese dopant but still retards the interfacial intermetallic growth compared to SnAg and SAC305. SnAg initially forms the thickest layer after reflow. After aging for 1000hr SnAg and SAC305 feature the thickest interfacial intermetallic layers.

5.1.1 Intermetallic Evolution as a result of Isothermal Aging at 185°C

In addition to nominally measuring the intermetallic layer thickness, the layer compositions were assessed and changes in morphology noted. Additionally, the microstructure of the solder bulk was also viewed.

In Figure 15, the ENIG plated copper pad and SnAg solder joint is displayed. The interfacial intermetallic layer is a combination of copper and nickel reacting with tin to form $(Cu,Ni)_6Sn_5$ with copper coming from the gullwing lead wire. The initial microstructure has fine Ag_3Sn particles dispersed in the bulk solder, after aging for 1000 hours these Ag_3Sn particles coalesce and increase in size.

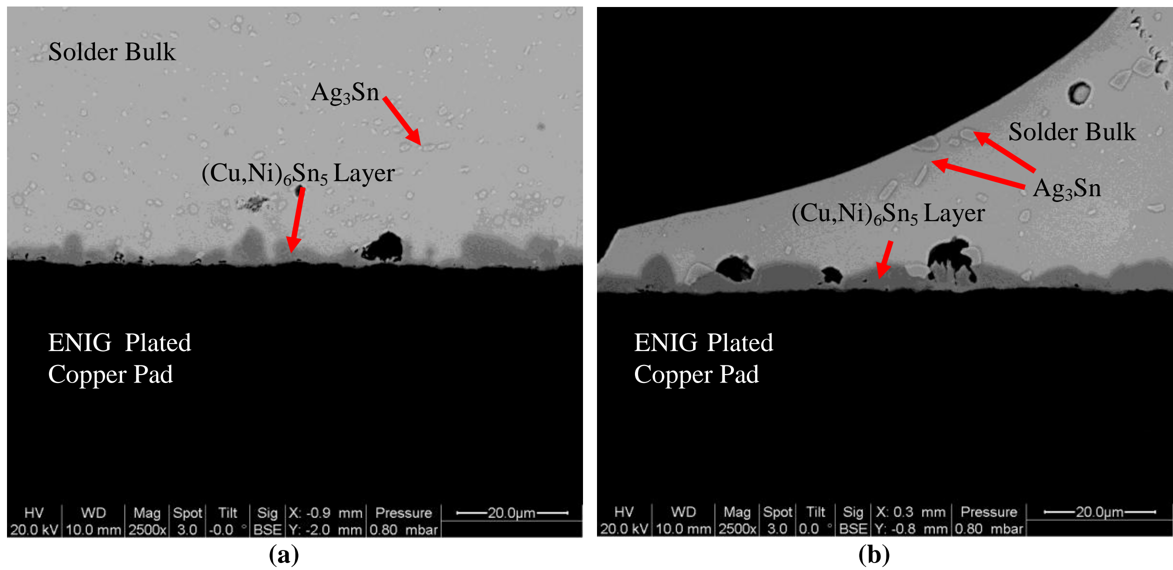


Figure 15: SnAg QFP solder joints, (a) after reflow, (b) after 1000 hours of aging at 185°C (courtesy CALCE).

Figure 16 shows the SAC305 QFP solder joints on the ENIG plated copper pad. Initially, very fine Ag_3Sn particles are well distributed within the solder bulk acting as a strengthening matrix. Cu_6Sn_5 particles are also found in the initial bulk solder. Additionally, the initial $(Cu,Ni)_6Sn_5$ interfacial intermetallic layer is very thin. After aging this layer develops large scallops that greatly increase the average thickness. Also, the very fine Ag_3Sn particles combine into fewer but larger intermetallics with some migrating toward the interfacial intermetallic surface.

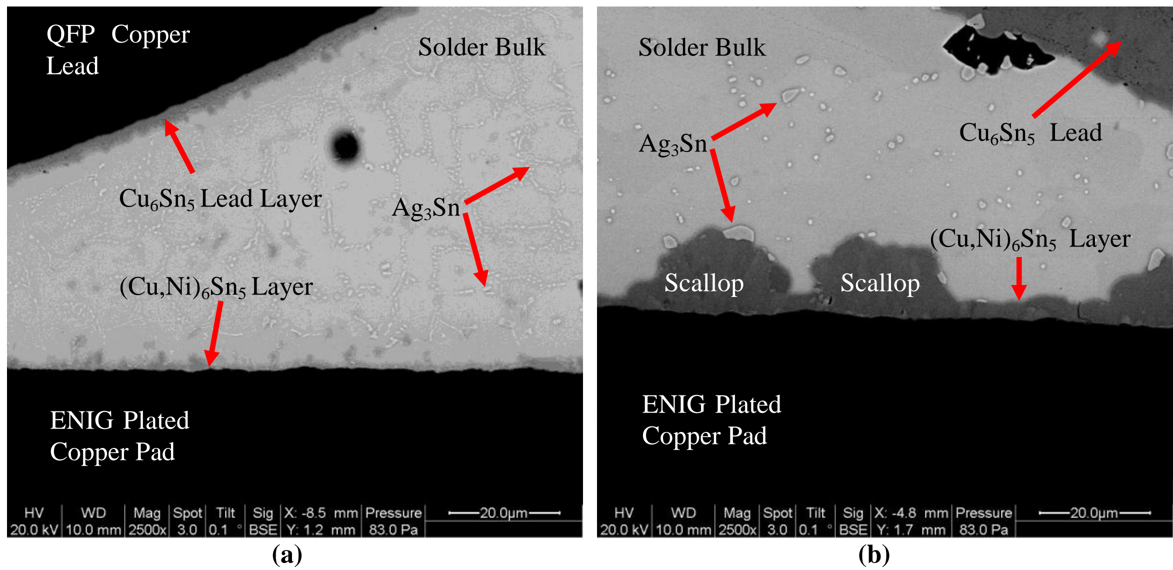


Figure 16: SAC305 QFP solder joints, (a) after reflow, (b) after 1000 hours of aging at 185°C (courtesy CALCE).

In Figure 17 the QFP SAC+Mn solder joint aging evolution is shown. Initially, the bulk solder has many Ag_3Sn and Cu_6Sn_5 particles that are well dispersed. The interfacial $(Cu,Ni)_6Sn_5$ layer is very thin but comparable to SAC305. After 1000 hours of aging very large Ag_3Sn and Cu_6Sn_5 are intermetallics are present in the bulk structure. These large intermetallics in the bulk lend themselves to potential failure sites through the bulk solder and could be a reliability risk. After aging interfacial $(Cu,Ni)_6Sn_5$ layer is much thinner than SAC305 with smaller and fewer scallop structures. The suppression of the interfacial intermetallic layer due to the manganese dopant is evident by this reduction in overall thickness compared to SAC305 and SnAg.

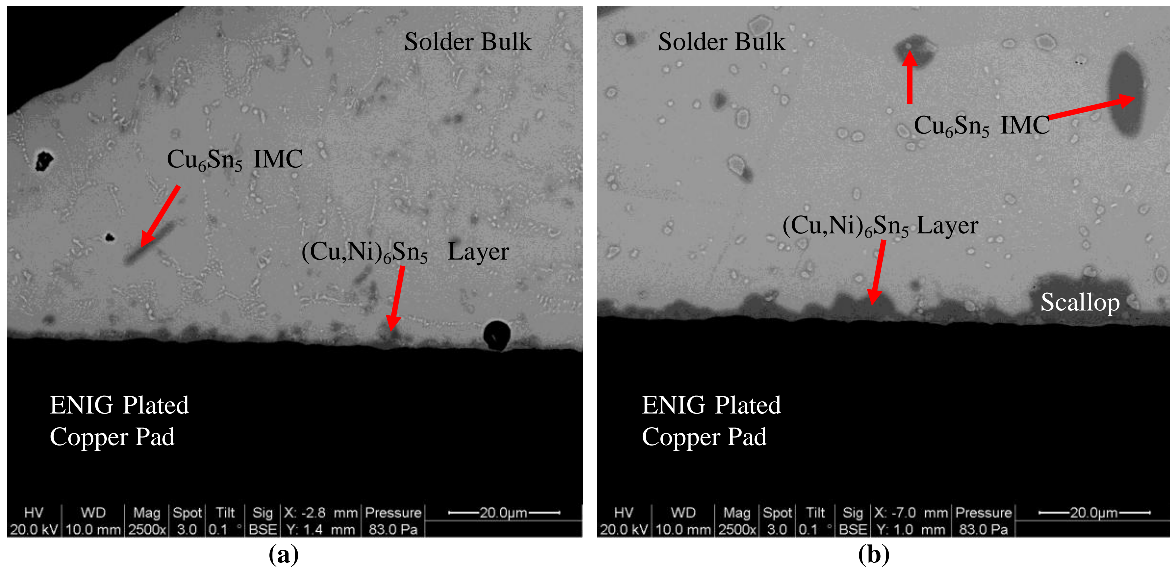


Figure 17: SAC+Mn QFP solder joints, (a) after reflow, (b) after 1000 hours of aging at 185°C (courtesy CALCE).

Figure 18 shows the SnAg+Cu Nano solder alloy on ENIG plated copper. Similar to SAC+Mn, the bulk solder joint develops Ag_3Sn and Cu_6Sn_5 intermetallics. After aging these intermetallics do not grow as large as the intermetallics in the SAC+Mn bulk. The $(Cu,Ni)_6Sn_5$ interfacial intermetallic layer initially is very thin and grows slowly. Scallop structures are rarer with a more continuous intermetallic layer than the SAC305 or SAC+Mn. Although, voiding is more prevalent in this solder alloy. As shown in the figure below, voids can exist at the end of the solder joint or near the interfacial intermetallic layer. Voids were also found in the bulk but are not shown in the images below.

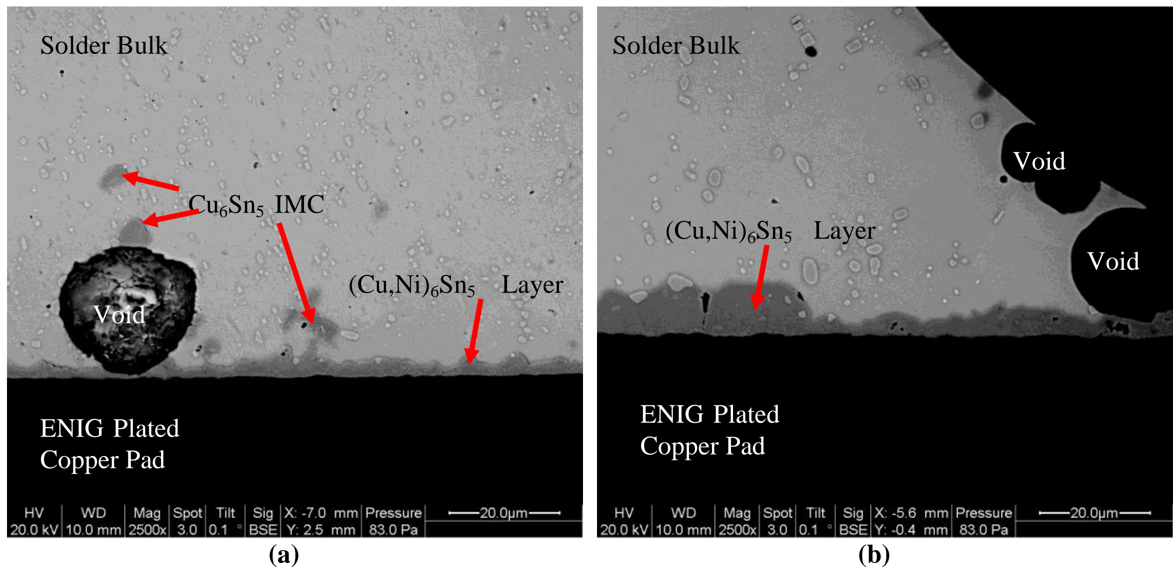


Figure 18: SnAg+Cu Nano QFP solder joints, (a) after reflow, (b) after 1000 hours of aging at 185°C (courtesy CALCE).

The interfacial intermetallics layers developed in QFP packages showed that the novel solders, SAC+Mn and SnAg+Cu Nano, suppress the interfacial intermetallic layers. The novel solders and SAC305 had both Ag_3Sn and Cu_6Sn5 intermetallics in the bulk structure, whereas SnAg only developed Ag_3Sn particles in the bulk.

5.2 200°C Aging Results QFP Samples

In addition to isothermal aging at 185°C, samples were isothermally aged at 200°C for 0, 100, 300 and 500 hours. Similarly, QFPs were removed after each aging interval and cross sectioned in order to measure the interfacial intermetallic layer and assess the bulk solder. In Figure 19, the results of the average intermetallic layer thickness are summarized.

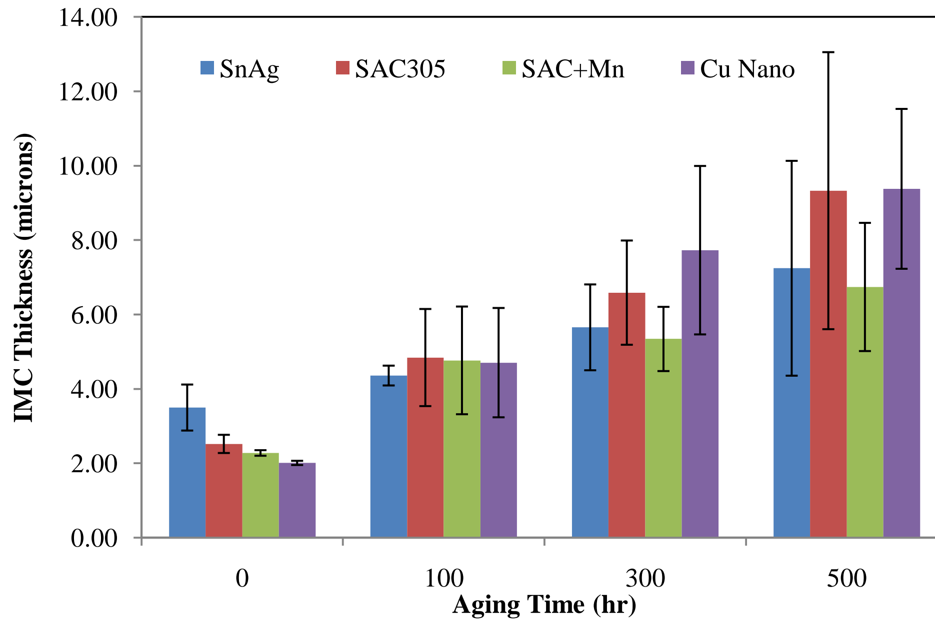


Figure 19: QFP interfacial intermetallic layer thickness results aged at 200°C up to 500 hours.

Similar trends from the 185°C are shown in the 200°C aging test. The SAC+Mn retards the intermetallic layer growth at the interface the best but does thicken at a higher temperature when compared to the 185°C results. Also, SAC305 grows rapidly and has the thickest intermetallic layer after aging. SnAg does not grow as fast compared to SAC305.

More interesting, the copper nano particle addition in SnAg does not appear to be an effective addition at 200°C. After 300 hours of aging the SnAg+Cu Nano has the thickest interfacial intermetallic layer. It is believed at this temperature, the diffusivity of copper is so high that the nano particles do not affect the diffusion of copper that is available from the copper QFP lead. Also, the copper nano particles migrate toward the interface to form intermetallic compounds as well. Therefore, the addition of copper nano particles is less effective at the suppression of the intermetallic layer at 200°C with copper leaded components.

5.2.1 *Intermetallic Evolution as a result of Isothermal Aging at 200°C*

Figure 20 displays the SnAg QFP solder joints near the end of the fillet. The initial intermetallic layer is quite thick but tends to grow slowly. Similar to the 185°C results, the initial microstructure has Ag_3Sn intermetallics dispersed in the bulk solder. After aging for 500 hours at 200°C, these Ag_3Sn particles are fewer but larger in size.

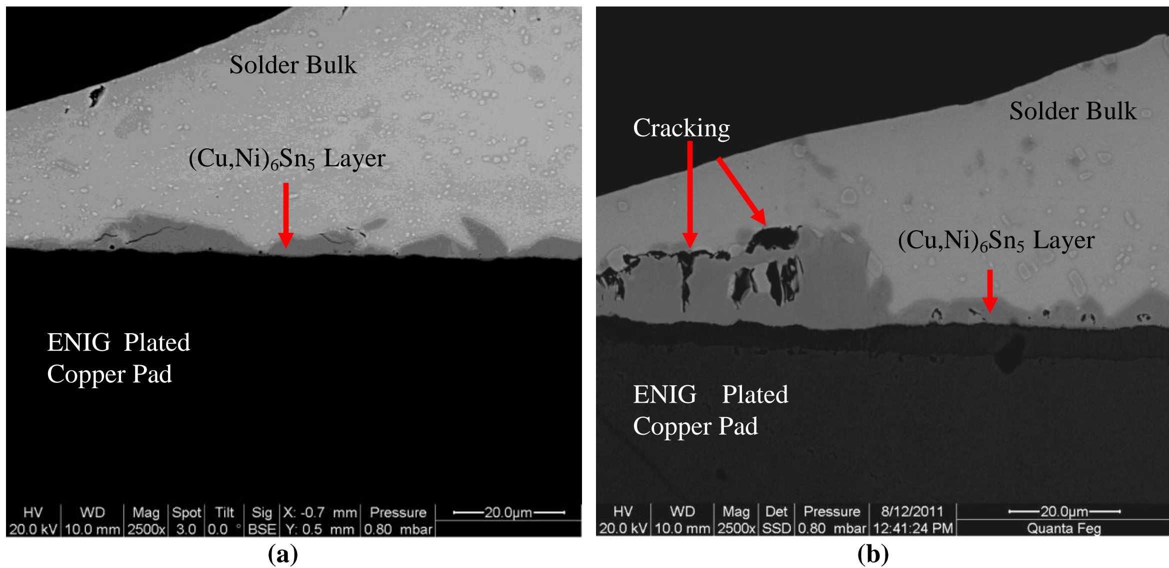


Figure 20: SnAg QFP solder joints, (a) after reflow, (b) after 500 hours of aging at 200°C (courtesy CALCE).

Figure 21 displays the SAC305 QFP solder joints aged at 200°C for 0 and 500 hours. The initial reflow is similar to the 185°C sample with fine Ag_3Sn and Cu_6Sn_5 intermetallic particles in the bulk. After aging, these particles tend to increase in size and Ag_3Sn particles can migrate towards the interface. The $(Ni,Cu)_6Sn_5$ intermetallic layer reacts similarly as the 185°C results. After 500 hours of aging very large scallops develop that are even bigger than the scallops observed after 1000 hours of aging at 185°C. Between large scallops a much thinner $(Ni,Cu)_6Sn_5$ layer connects the scallops explaining the large variation in this intermetallic layer measurement.

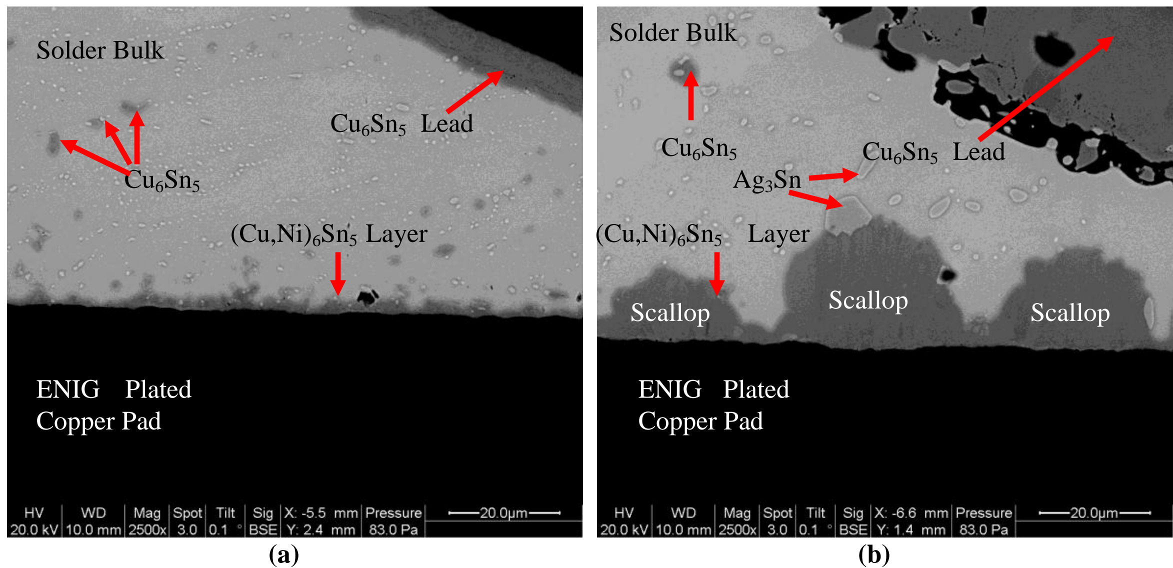


Figure 21: SAC305 QFP solder joints, (a) after reflow, (b) after 500 hours of aging at 200°C (courtesy CALCE).

In Figure 22 QFP solder joints utilizing the SAC+Mn alloy are shown. Similar to the results from the 185°C test, the bulk features many Ag_3Sn and Cu_6Sn_5 particles that are dispersed through the joint. After aging for 500 hours these particles are large but not as large as the particles present in the 185°C samples aged 1000 hours. The interfacial $(Cu,Ni)_6Sn_5$ layer follows a similar trend as the 185°C test, with a very thin initial layer and a suppressed layer after aging. The scallop structure seen in the SAC305 samples exists in the SAC+Mn but are much smaller and fewer. At 200°C the manganese dopant suppresses the interfacial intermetallic layer growth very well.

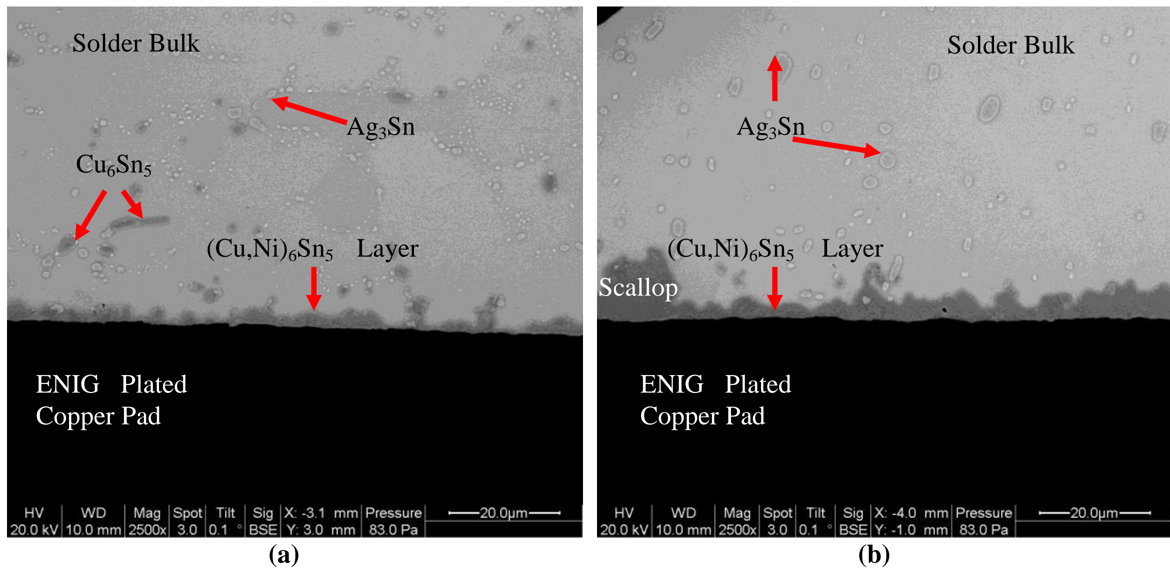


Figure 22: SAC+Mn QFP solder joints, (a) after reflow, (b) after 500 hours of aging at 200°C (courtesy CALCE).

Finally, in Figure 23 the QFP joints utilizing the SnAg+Cu Nano solder are shown. In these images it is very apparent large voids appear in these joints which pose a serious reliability threat. These voids may be artifacts of the flux used during reflow. Additionally, the oxidation on the copper nano particles may have reacted poorly with with the flux and created more voids than usual. Also, the impact of the copper nano particles at 200°C is not as effective suppressing the growth of interfacial intermetallics. The $(Cu,Ni)_6Sn_5$ layer, while tending to be more continuous, grows very thick after aging for 500 hours.

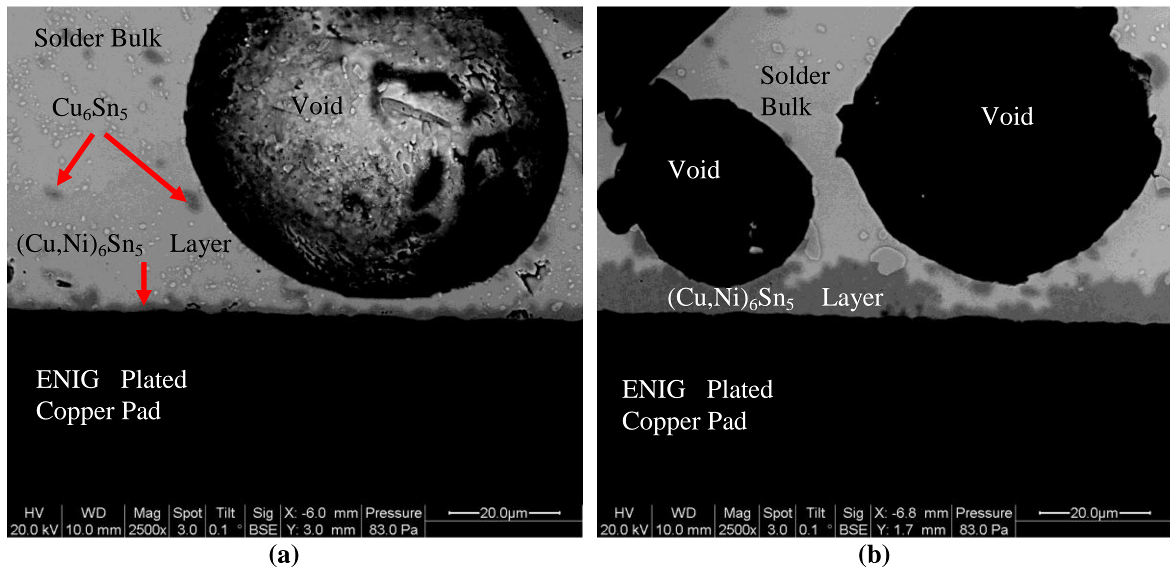


Figure 23: SnAg+Cu Nano QFP solder joints, (a) after reflow, (b) after 500 hours of aging at 200°C (courtesy CALCE).

5.3 200°C Aging Results 2512 Chip Resistor Samples

The results of the 200°C QFP samples led to questions about the usefulness of the copper nano particles. A study of the chip resistors aged at 200°C was performed to determine if the copper lead of the QFP components negatively affects the copper nano particle solder alloy performance. The intermetallic layer thickness data obtained from the 2512 chip resistors is very peculiar. The SAC+Mn and SnAg+Cu Nano suppress the interfacial intermetallic layer very well and appear to reach a stable thickness. The results of the SnAg+Cu Nano are noteworthy because the QFP joints did not see a positive effect of the copper nano particle addition. This is believed to be a result of the plentiful copper from the QFP lead that is no longer present with the nickel leaded chip resistors.

The SnAg and SAC305 samples have very rapid growth between 100 and 300 hours of aging. Inspection of these interfacial intermetallic layers reveals a strange phenomenon. The results of the thickness measurements are summarized in Figure 24.

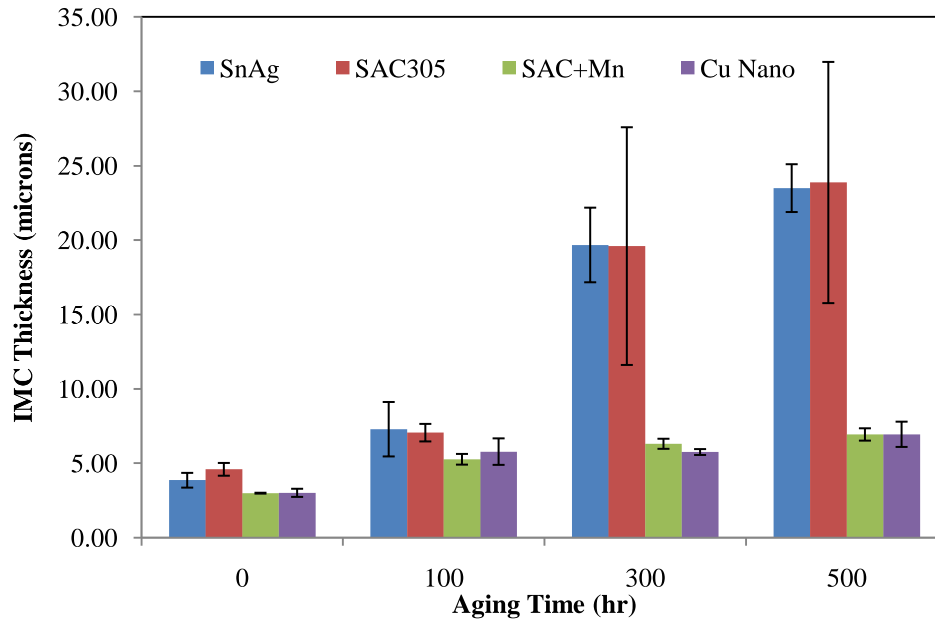


Figure 24: 2512 Chip resistors interfacial intermetallic layer thickness results aged at 200°C for a maximum of 500 hours.

It is obvious that another mechanism is driving the SnAg and SAC305 rapid interfacial intermetallic layer growth. The following subsection will present and explain the intermetallic layer evolution observed in this isothermal aging study.

5.4 Four Layer Intermetallic Layer Evolution

SnAg and SAC305 displayed a phenomenon in intermetallic layer growth not expected from the study. First, the evolution of the intermetallic layers will be discussed and then the intervals in which the evolution for SnAg and SAC305 occurs will be noted. Both solders exhibit similar growth patterns at the same aging intervals. In Figure 25, the evolution of the interfacial intermetallic layers for the two solders is shown. The columns in Figure 25 separate the solder type, SnAg on the left and SAC305 on the right, and the rows refer to the aging time at 200°C, starting from the top 0, 100, 300, and 500 hours respectively.

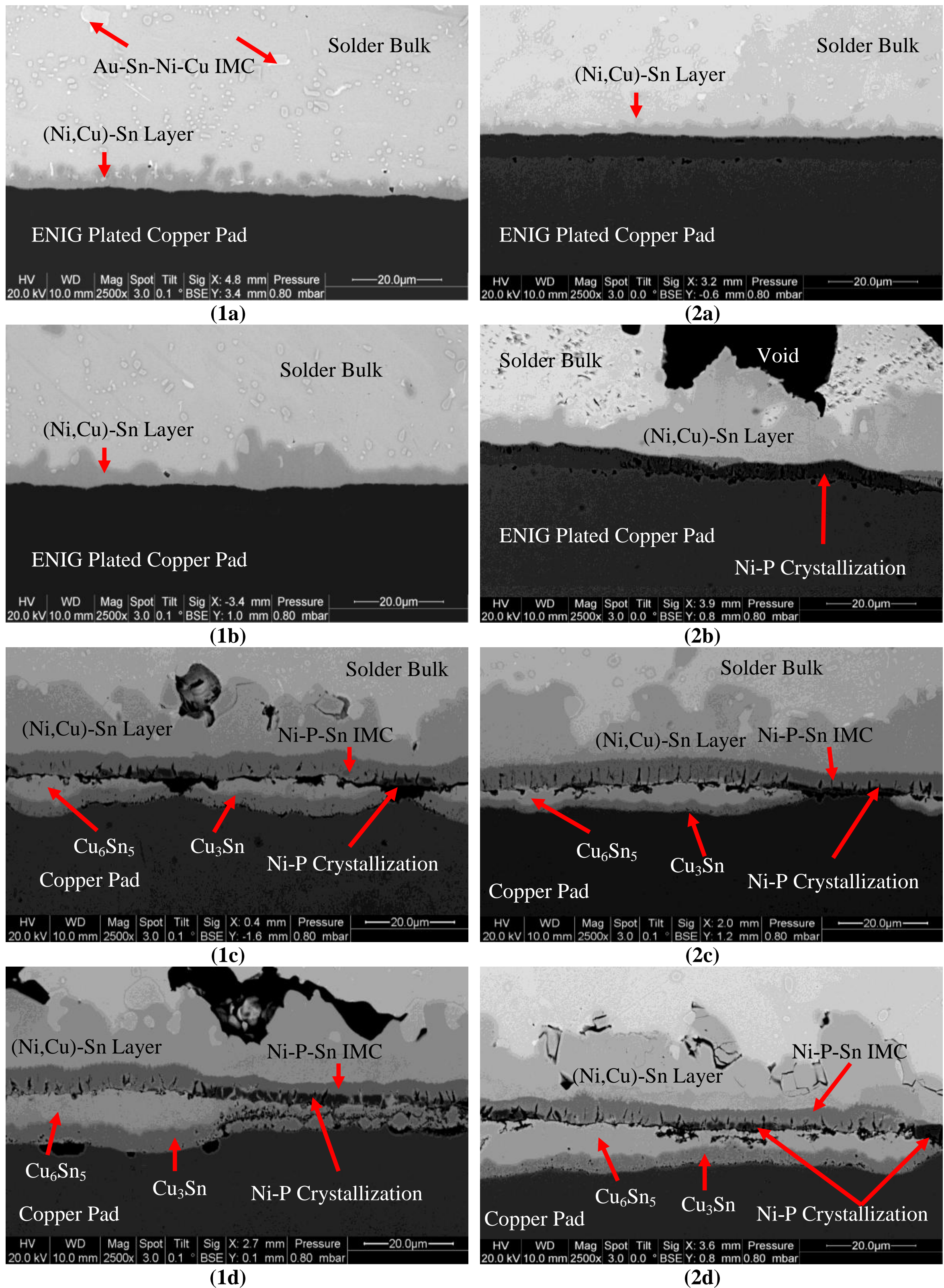


Figure 25: Intermetallic layer evolution of chip resistors aged at 200°C, (1a) SnAg 0hr aging, (2a) SAC305 0hr aging, (1b) SnAg 100hr aging, (2b) SAC305 100hr aging, (1c) SnAg 300hr aging, (2c) SAC305 300hr aging, (1d) SnAg 500hr aging, (2d) SAC305 500hr aging (courtesy CALCE).

The evolution of the nickel layer is responsible for this phenomenon. Initially, all joints show a uniform nickel layer between the copper pad and solder. During aging this nickel layer darkens, turning into a reaction layer. The reaction layer is a crystallization of the nickel and phosphorus, used during the electroless plating, which develops as nickel is consumed [19]. The reaction layer then transforms into a Ni-P-Sn intermetallic layer. After the nickel layer is completely consumed, the diffusion barrier no longer exists. Underneath the Ni-P-Sn intermetallic layer, two distinct copper intermetallic layers form. The layer just above the copper pad is Cu_3Sn and the layer between the Cu_3Sn and Ni-P-Sn intermetallic layer is Cu_6Sn_5. Without the nickel diffusion barrier, the four intermetallic layers grow very rapidly as seen in Figure 24.

SnAg and SAC305 exhibit the transformation at the same intervals. Initially just after reflow, a full nickel layer is viewed with a thin reaction layer between the nickel and nickel intermetallic layer. After 100 hours of aging, the reaction layer begins to grow at various locations but not uniformly. After 300 hours of aging, the reaction layer transforms into the Ni-P-Sn intermetallic layer and forms pockets where the transformation is complete allowing for two additional copper intermetallic layers to form, consuming the copper pad. Finally, after 500 hours of aging, the pockets begin to merge and form layers. It is noteworthy to point out that trend is not continuous and will have some sections without the phenomenon occurring, thus the large uncertainty of the average interfacial intermetallic layer thickness.

The formation of four intermetallic layers is not an occurrence unique to this test. The phenomenon was recently reported by Yoon et al, studying SnAg and SAC387 [68]. This

study utilized chip resistors with nickel leads, ENIG finish copper pads, and aging at 200°C. The results are very similar to the results shown in this experiment.

5.5 Discussion of Isothermal Aging Study

Several interesting results were obtained from the isothermal aging study. First, the manganese dopant in a SAC alloys suppressed the interfacial intermetallic layer very well for both copper and nickel component terminations. SnAg+Cu Nano has reasonable success slowing the intermetallic layer growth. At 185°C with copper leaded QFP components and with nickel termination chip resistors the copper nano particle addition suppressed the intermetallic layer growth. However, at 200°C with the QFP component the nano particle addition did not suppress the intermetallic layer. In general, SAC305 tends to form thicker intermetallic layers than SnAg after long term aging. Finally, the chip resistors revealed a nickel consumption phenomenon resulting in the formation of four intermetallic layers. The impact on reliability of the four intermetallic layer structure is unknown since five interfaces between layers now exist offering potential for a weak link that could cause failure.

After the isothermal aging test, a durability thermal and vibration cycling test was performed on test boards isothermally aged to the same conditions as this study. The results of the reliability test will be discussed in the next chapter.

Chapter 6: Thermal/Vibration Cycling Durability Test

The combined thermal and vibration cycling durability testing was split into two tests based on pre-isothermal aging temperature that corresponded to the maximum thermal cycling temperature. The tests consisted of 200 thermal cycles and one million 50G vibration cycles in each of the three axes. After pre-isothermal aging, the test boards were tested in intervals of 50 thermal cycles and then 250,000 vibration cycles in each of the three axes. A total of four testing intervals were used to complete the entire testing protocol.

6.1 Test One Durability Results

Test one consisted of pre-isothermal aging at 185°C for 0, 100, 300, and 1000 hours followed by the durability testing using a thermal cycle range from -40°C to 185°C intermixed with 50G vibration cycling.

6.1.1 -40°C to 185°C Thermal/Vibration Cycling

In order to tabulate the time to failure, thermal cycles were used as the time parameter, noting that vibration cycling occurred after every 50 thermal cycles. Thermal cycles are easy to track time to failure due to the length of each cycle. Vibration cycling frequency was in excess of 500Hz; the ANATech STD 256 could not produce a sampling rate of 5000Hz necessary to avoid aliasing, thus the exact cycle a failure occurred could not be determine. Rather monitoring determined if the failure occurred during the vibration cycling. Failures during vibration cycling were associated as a 50th, 100th, 150th or 200th thermal cycle failure.

Failures determined during thermal cycling by the ANATech were always recorded as failures, however the uniaxial shaker creates electromagnetic fields that can induce a current in the monitoring wires and potentially cause a false failure. To avoid this potential source of error, the monitoring wires were wrapped in an aluminum sheath. Additionally, failures detected during vibration cycling were validated by a resistance measurement using a voltmeter. If the failure was verified it was recorded, however two cases arose where the failure was not verified. A failure can potentially not be detected when not in the harsh environment, thus these two cases were noted as potential failures and returned to the thermal cycling. If the failure was detected within five thermal cycles, the failure was considered a vibration cycling failure, which occurred in both cases.

The durability results of the QFP and chip resistor chains are summarized in Table 4 and Table 5 respectively. The QFP components rarely, if ever failed during the prescribed testing. This result confirms the good performance of lead free solders in small leaded devices but does little to differentiate the solder alloy performance. The compliant QFP gullwing shaped lead carries a portion of the thermal expansion mismatch strain thus reducing the strain on the solder joint. The availability of copper that dissolves into the solder during reflow allows for copper based $(Cu,Ni)_6Sn_5$ intermetallic layers to form which are less brittle than the nickel based intermetallics.

Table 4: QFP failure results -40°C to 185°C thermal cycling and vibration cycling

QFP Failures								
	SnAg				SAC 305			
Cycles	0hr	100hr	300 hr	1000 hr	0hr	100hr	300 hr	1000 hr
1 to 50	0/4	0/4	0/4	0/4	0/4	0/4	0/4	0/4
51 to 100	0/4	0/4	0/4	0/4	0/4	0/4	0/4	0/4
101 to 150	0/4	0/4	0/4	0/4	0/4	0/4	0/4	0/4
151 to 200	0/4	0/4	0/4	0/4	0/4	0/4	0/4	0/4
	SAC + Mn				Sn-Ag + Cu Nano			
Cycles	0hr	100hr	300 hr	1000 hr	0hr	100hr	300 hr	1000 hr
1 to 50	0/4	0/4	0/4	0/4	0/4	0/4	0/4	0/4
51 to 100	0/4	0/4	0/4	0/4	0/4	0/4	0/4	0/4
101 to 150	0/4	0/4	0/4	0/4	0/4	1/4	0/4	1/4
151 to 200	0/4	0/4	0/4	0/4	0/4	1/4	0/4	1/4

Legend: **Green**=No Failures, **Yellow**=One Failure, **Orange**= 2-3 Failures **Red**=All Failed

The large 2512 chip resistors were utilized in order to induce more failures that would allow for differentiation amongst the solder selections. The 2512 chip resistors have no strain reliving system and the alumina substrate of the chip resistor has a very small coefficient of thermal expansion, thus creating large thermal expansion mismatch strain. Additionally, the nickel leaded resistors create a nickel based $(Ni,Cu)_3Sn_4$ intermetallic layer on the resistor termination. This brittle intermetallic is likely to cause failures more rapidly than a copper based intermetallic.

Table 5: 2512 chip resistors failure results -40°C to 185°C thermal cycling and vibration cycling

2512 Chip Resistor Failures								
	SnAg				SAC 305			
Cycles	0hr	100hr	300 hr	1000 hr	0hr	100hr	300 hr	1000 hr
1 to 50	0/4	0/4	0/4	0/4	0/4	0/4	0/4	0/4
51 to 100	0/4	0/4	0/4	0/4	0/4	0/4	0/4	0/4
101 to 150	1/4	1/4	2/4	0/4	0/4	0/4	1/4	0/4
151 to 200	1/4	1/4	2/4	0/4	1/4	1/4	1/4	1/4
	SAC + Mn				Sn-Ag + Cu Nano			
Cycles	0hr	100hr	300 hr	1000 hr	0hr	100hr	300 hr	1000 hr
1 to 50	0/4	0/4	0/4	1/4	0/4	1/4	0/4	0/4
51 to 100	0/4	1/4	1/4	3/4	0/4	1/4	2/4	0/4
101 to 150	1/4	1/4	1/4	3/4	0/4	1/4	2/4	1/4
151 to 200	1/4	1/4	1/4	3/4	1/4	2/4	3/4	3/4

Legend: **Green**=No Failures, **Yellow**=One Failure, **Orange**= 2-3 Failures **Red**=All Failed

The novel solders have poorer performance than SnAg and SAC305 despite a thinner interfacial intermetallic layer. It must be noted the SAC+Mn and SnAg+Cu Nano are research grade solder alloys that lack the process and production control of the commercialized SnAg and SAC305 alloys. The control of the alloying process and the optimized reflow parameters of the commercial solders expect better joint formation. However, detailed failure analysis will be required to assess the reasons for the poor durability performance of the novel solders.

Table 6 shows the breakdown of failures occurrence, either during thermal cycling or vibration cycling. Thermal cycling accounts for about two thirds of all failures, but the fraction of thermal cycle failures is affected by the higher rate of vibration failures in the SnAg+Cu Nano solder alloy.

Table 6: Test 1 chip resistor failure occurrence by testing method and solder type.

	Total	SnAg	SAC305	SAC+Mn	Cu Nano
Thermal	17	3	3	5	6
Vibration	7	1	1	1	4
Total	**24**	**4**	**4**	**6**	**10**

Additionally, the failure data can be divided according to the chip resistor chain location on the test boards. Applying the numbering scheme shown in Figure 26, the failure data can be divided by location on the test board.

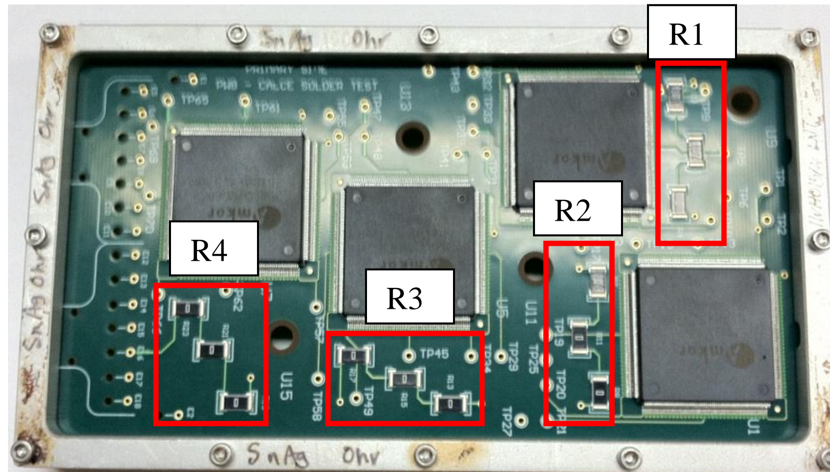


Figure 26: Test board chip resistor chain number scheme.

In Table 7, the breakdown of failures according to the chip resistor chain location on the test board is summarized. Locations R2 and R3 account for ~71% of all failures, indicating vibration cycling impart significant damage to the solder joints since R2 and R3 experience the highest G force due to their location closest to the center of the test board. The amount of time spent thermal cycling versus time spent on the shaker table could account for the greater percentage of failures occurring during thermal cycling despite the indication that vibration cycling is impacting the failure location.

Table 7: Test 1 failure by location on test board and solder type.

	Total	SnAg	SAC305	SAC+Mn	Cu Nano
R1	4	1	0	1	2
R2	7	1	1	2	3
R3	10	2	2	3	3
R4	3	0	1	0	2
Total	24	4	4	6	10

6.1.2 QFP Intermetallic Layer Thickness Comparison

After the full set of thermal and vibration cycling was completed for test one, a QFP was removed and cross sectioned to assess the interfacial intermetallic layer thickness. In Figure 27, the results of the isothermal aging intermetallic layer thickness are compared with the results for each pre-isothermal aging condition after durability testing.

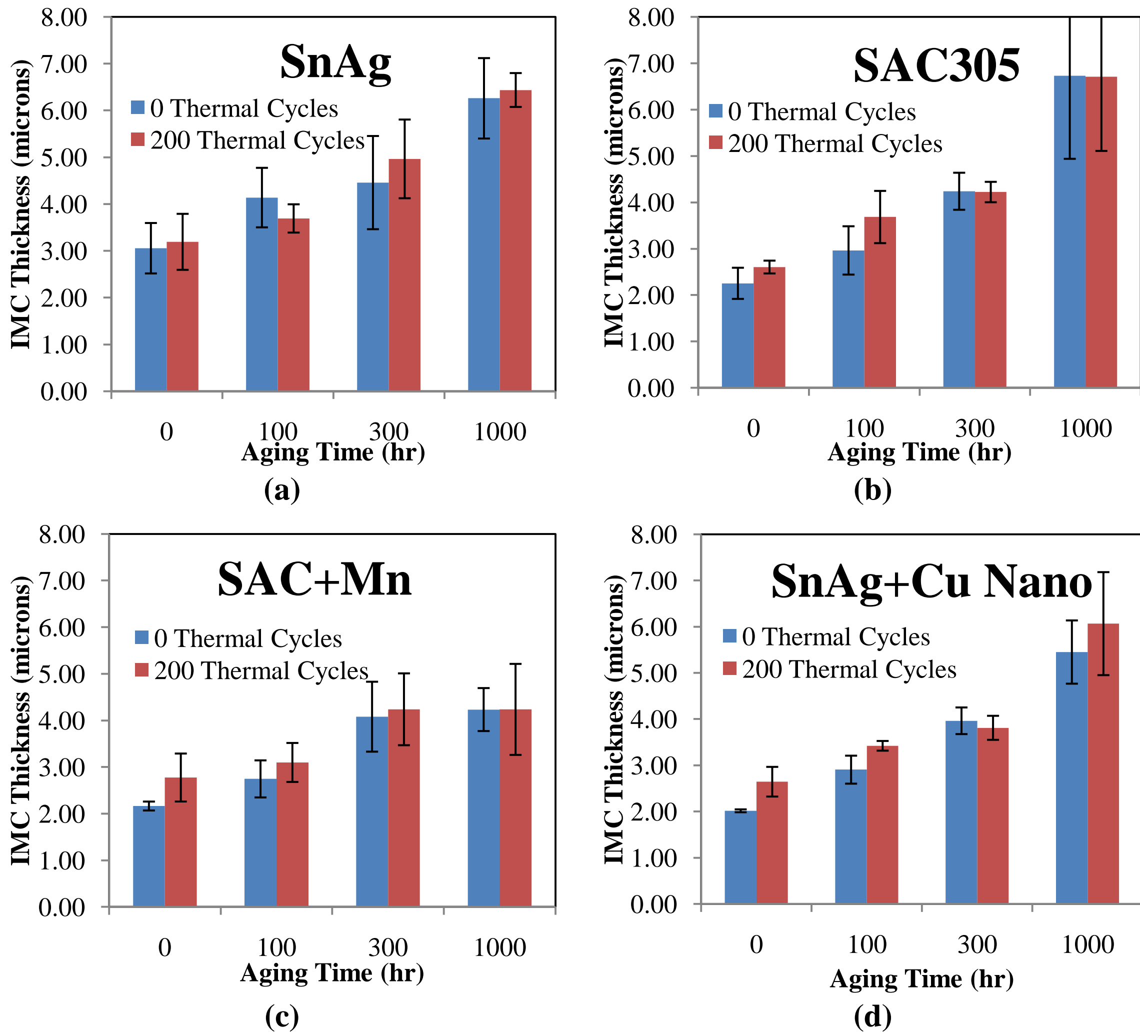


Figure 27: Comparison of QFP interfacial intermetallic layer thickness before and after thermal/vibration cycling for each solder and isothermal aging condition at a maximum of 185°C.

There is little difference in the intermetallic layer thickness after durability testing for each aging condition. This can be explained by the short amount of time at the maximum temperature of 185°C and that the average temperature during cycling is only 84.26°C. It is interesting to note a few cases nominally show a decrease in thickness after cycling; however the uncertainty of the measurements overlaps any examples.

6.2 Test Two Durability Results

In test two, the test boards were aged before testing at 200°C for 0, 100, 300, and 500 hours, then subjected to the durability testing protocol with a thermal cycle range of -40°C to 200°C intermixed with one million 50G vibration cycles in each axis.

6.2.1 -40°C to 200°C Thermal/Vibration Cycling

The durability results from test two are very similar to the results from test one. The results of the QFP failures and the 2512 chip resistors are summarized in Table 8 and Table 9 respectively. Again, nearly no QFP components experienced solder joint failure. Only one QFP failure was observed amongst 64 QFPs that were tested, providing no differentiation between solders even at the higher cycling temperature.

Table 8: QFP failure results -40°C to 200°C thermal cycling and vibration cycling

QFP Failures								
	SnAg				SAC 305			
Cycles	0hr	100hr	300 hr	500 hr	0hr	100hr	300 hr	500 hr
1 to 50	0/4	0/4	0/4	0/4	0/4	0/4	0/4	0/3
51 to 100	0/4	0/4	0/4	0/4	0/4	0/4	0/4	0/3
101 to 150	0/4	0/4	0/4	0/4	0/4	0/4	0/4	0/3
151 to 200	0/4	0/4	0/4	0/4	0/4	0/4	0/4	0/3
	SAC + Mn				Sn-Ag + Cu Nano			
Cycles	0hr	100hr	300 hr	500 hr	0hr	100hr	300 hr	500 hr
1 to 50	0/4	0/4	0/4	0/4	0/4	0/4	0/4	0/4
51 to 100	0/4	0/4	1/4	0/4	0/4	0/4	0/4	0/4
101 to 150	0/4	0/4	1/4	0/4	0/4	0/4	0/4	0/4
151 to 200	0/4	0/4	1/4	0/4	0/4	0/4	0/4	0/4

Legend: **Green**=No Failures, **Yellow**=One Failure, **Orange**= 2-3 Failures **Red**=All Failed

The second test chip resistors produced more rapid failure rates than the first test. Three different conditions produced full sets of failures for the 2512 chip resistor chains. Test one did not produce a full set of failures of any component. The novel solders often produced failures very early, which could indicate a different failure mechanism.

Table 9: 2512 chip resistors failure results -40°C to 200°C thermal cycling and vibration cycling

2512 Chip Resistor Failures								
	SnAg				SAC 305			
Cycles	0hr	100hr	300 hr	500 hr	0hr	100hr	300 hr	500 hr
1 to 50	0/4	0/4	0/4	0/4	0/4	0/4	0/4	0/4
51 to 100	0/4	0/4	1/4	0/4	0/4	0/4	0/4	0/4
101 to 150	2/4	0/4	1/4	0/4	0/4	0/4	0/4	0/4
151 to 200	3/4	1/4	3/4	1/4	1/4	1/4	0/4	1/4
	SAC + Mn				Sn-Ag + Cu Nano			
Cycles	0hr	100hr	300 hr	500 hr	0hr	100hr	300 hr	500 hr
1 to 50	0/4	1/4	2/4	2/4	0/4	0/4	0/4	2/4
51 to 100	0/4	1/4	3/4	4/4	0/4	1/4	0/4	3/4
101 to 150	0/4	1/4	3/4	4/4	3/4	1/4	1/4	3/4
151 to 200	0/4	1/4	4/4	4/4	3/4	1/4	1/4	4/4

Legend: **Green**=No Failures, **Yellow**=One Failure, **Orange**= 2-3 Failures **Red**=All Failed

Both test showed that SnAg and SAC305 were superior in regard to durability than either of the novel solders. SAC305 outperformed SnAg in both tests in these studies' experimental conditions. The failure analysis and shear testing results are required to determine the reasons for the unexpected failure results produced by the two tests.

The breakdown of failure induced by testing type is summarized in Table 10. About 75% of failures are induced by thermal cycling.

Table 10: Test 2 chip resistor failure occurrence by testing method and total failures.

	Total	SnAg	SAC305	SAC+Mn	Cu Nano
Thermal	22	6	2	6	8
Vibration	7	2	1	3	1
Total	29	8	3	9	9

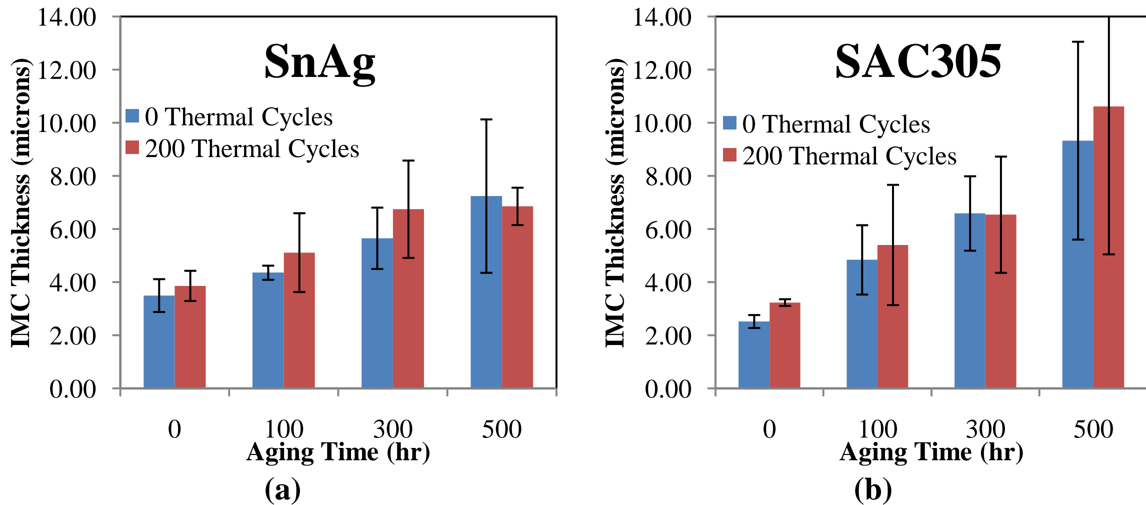
Failures were also classified by location according to the chain labeling shown in Figure 26. The results are summarized in Table 11. Locations R2 and R3 account for 55% of all failures in test two as compared to 71% of failures in test one. This indicates that the increased strain due to the higher temperature range is inducing more failures during thermal cycling in this test.

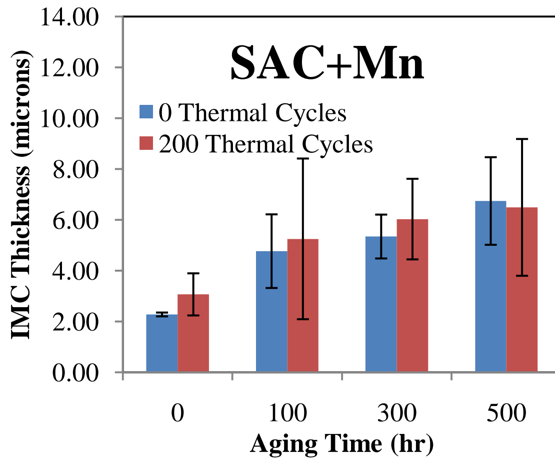
Table 11: Test 2 failure by location on test board and solder type.

	Total	SnAg	SAC305	SAC+Mn	Cu Nano
R1	6	1	0	2	3
R2	6	2	0	2	2
R3	10	2	3	3	2
R4	7	3	0	2	2
Total	29	8	3	9	9

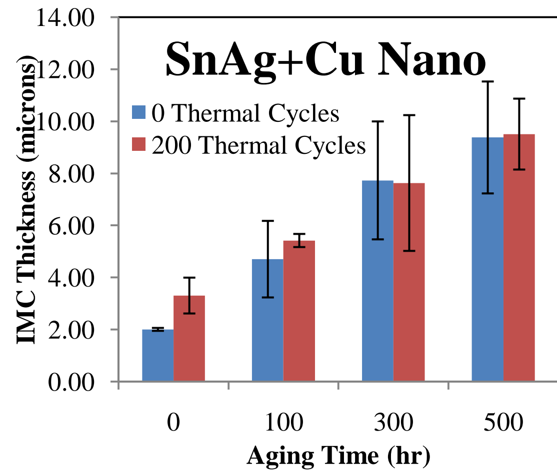
QFP Intermetallic Layer Thickness Comparison

Similar to test one, the QFP interfacial intermetallic layer was measured at the conclusions of testing. Again, thermal cycling did not greatly impact the average thickness. A summary of these results compared to the isothermal aging thickness measurements are summarized in Figure 28. Even at the more extreme cycling temperature in test two, the average temperature during cycling was only 91.93°C, far below the 200°C aging condition. Thus, minimal increases were observed during thermal cycling.





(c)

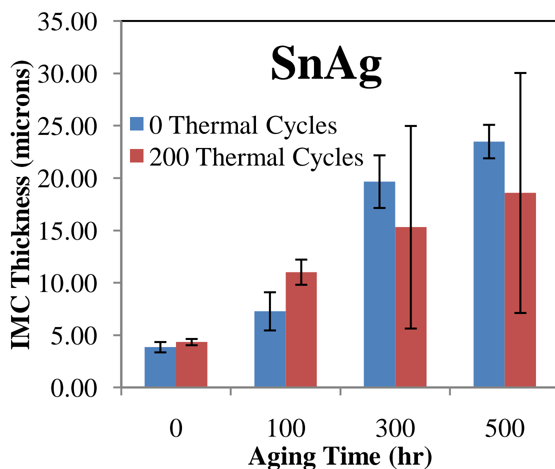


(d)

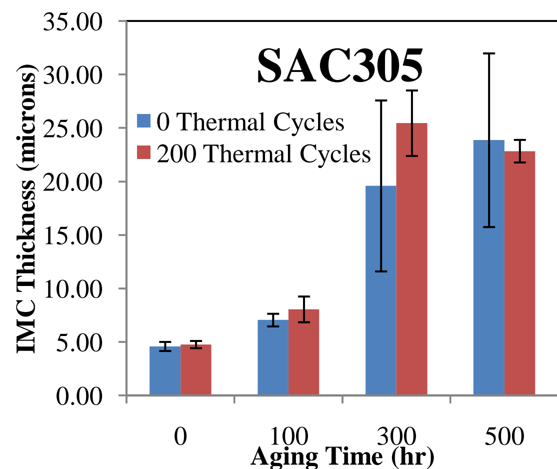
Figure 28: Comparison of QFP interfacial intermetallic layer thickness before and after thermal/vibration cycling for each solder and isothermal aging condition at a maximum of 200°C.

6.2.2 2512 Chip Resister Intermetallic Layer Thickness Comparison

In addition to measuring the interfacial intermetallic layer thickness of the QFP components, in test two the measurements were also performed on the chip resistors. In Figure 29, the interfacial thicknesses are compared with the isothermal aging measurements.



(a)



(b)

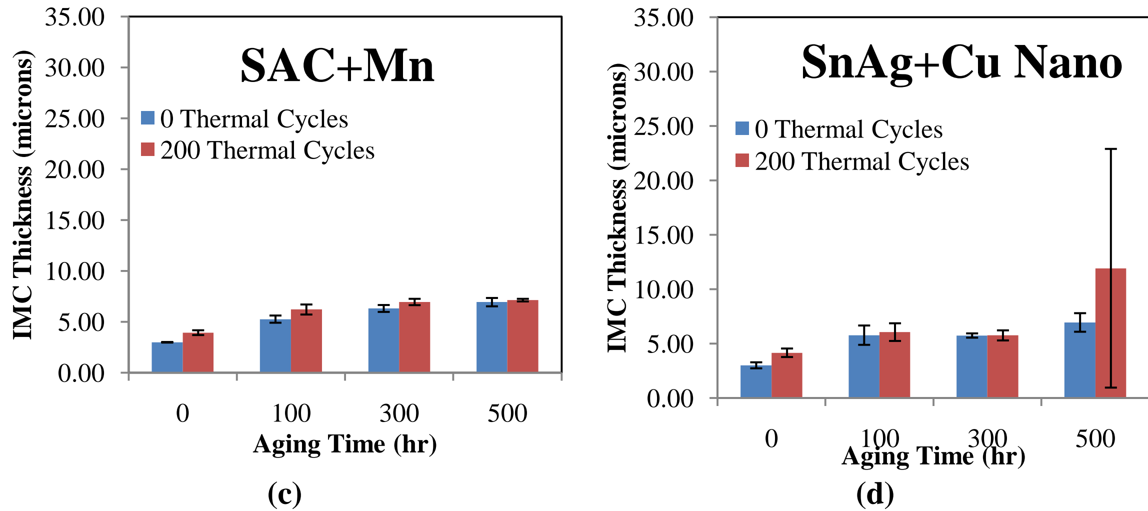


Figure 29: Comparison of 2512 chip resistor interfacial intermetallic layer thickness before and after thermal/vibration cycling for each solder and isothermal aging condition at a maximum of 200°C.

Unlike the QFP measurements several interesting effects were deduced from the measurements of the chip resistors after durability testing. First, the SnAg+Cu Nano interfacial intermetallic layer appeared to stabilize after 100 hours during the isothermal aging test. However, the 500 hour aging sample experienced renewed growth during thermal cycling. In fact, the SnAg+Cu Nano experienced the nickel layer consumption effect that SnAg and SAC305 displayed, as discussed in Chapter 5. SnAg+Cu Nano, does not transform as rapidly as SnAg and SAC305. After 500 hours of aging and thermal cycling, the phenomenon begins forms in small regions dispersed across the solder joint. The reactions follow the same evolution as previously discussed but at a slower rate. This is believed to be caused by the same mechanism that limits the intermetallic layer growth. The copper nano particles pin the grain boundaries and slow diffusion requiring more time for the phenomenon to occur due to slower consumption of nickel.

One other noteworthy observation can be made from this data. Both SnAg and SAC305 show high level of variation during the formation of the four intermetallic layer structure

discussed in Chapter 5. This indicates that the formation does not occur uniformly. The SnAg isothermal aging results indicate less variation than SAC305 however after isothermal aging and thermal cycling the opposite is true. Further study is required to understand this phenomenon, its affect on solder joint reliability, and the growth model.

6.3 Failure Analysis

Due to the lack of QFP failures, only chip resistors were inspected for failure analysis. The cross sections of the chip resistor joints were viewed to find the failure initiation, crack location, and pathway. Additionally, alternate failure mechanisms for SAC+Mn and SnAg+Cu Nano were explored in an attempt to explain the poor durability results.

6.3.1 Failure Locations and Pathway

The location of the initiation of failures and interface of the cracks were determined first. Failures were only observed at the chip level and not at the copper pad level. The chip resistor cracks initiate at two locations, the corner of the resistor termination and at the end of the termination that is below the resistor. In Figure 30a, the crack that initiates at the end of the lead is shown along with the crack initiating at the corner in Figure 30b.

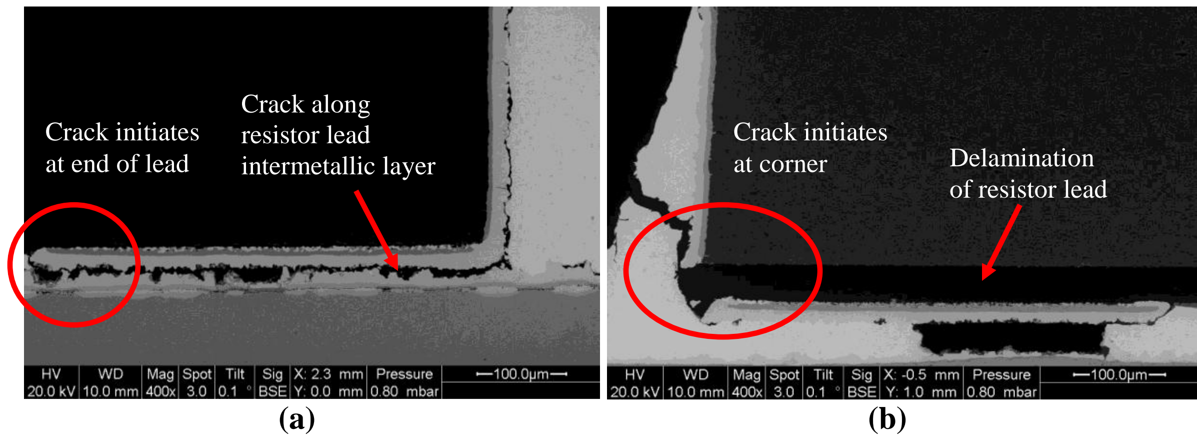


Figure 30: Failure site initiation and layer, (a) SAC305 aged 300hr at 200°C and full set of thermal/ vibration cycling, (b) SnAg aged 300hr at 200°C and full set of thermal/vibration cycling (courtesy CALCE).

In addition to initiating, the interface the crack fractures along was also noted. Two crack locations were observed. First, the fracture was between the resistor termination intermetallic layer and the solder underneath the resistor as shown in Figure 30a. The other crack interface was between the chip resistor alumina substrate and the resistor termination. This failure location appeared to be a delamination of the chip resistor lead.

Delamination of the chip resistors is highly unexpected since surface mount chip resistors are expected to performed reliability at higher temperature than 200°C. Vibration cycling is potentially causing the delamination, however the time when a crack initiates cannot be determined from the failure data thus making it difficult to prove if vibration cycling is causing this failure location. Further research is required to determine if vibration cycling is causing this failure alone or if it is a combination of thermal and vibration cycling.

After cracking along the resistor lead, or if the failure initiated in the corner, two crack paths have been viewed. The crack can continue by following the chip lead intermetallic layer and cracking at the solder bulk interface or the crack will travel through the solder bulk. An example of each of this failure path is shown in Figure 31.

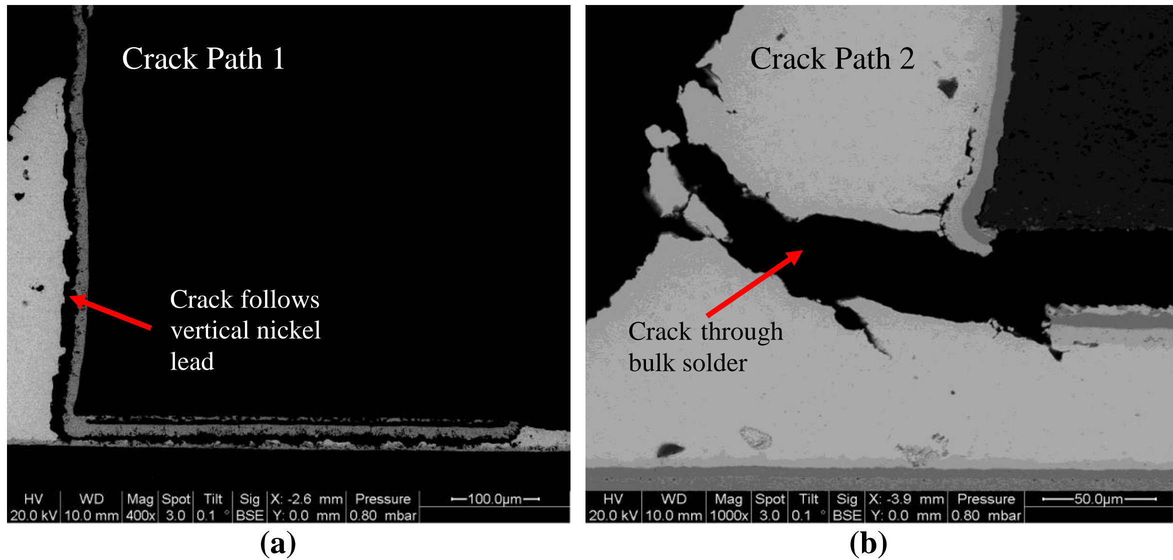


Figure 31: 2512 chip resistor failure pathway, (a) SAC+Mn aged 100hr at 200°C and full set of cycling, (b) SnAg+Cu Nano aged 100hr at 200°C and full set of cycling (courtesy CALCE).

Cracking along the chip resistor intermetallic layer and bulk solder interface is indicative of brittle failure, which was expected during the vibration cycling. The failure through the bulk is believed to be caused by thermal cycling.

6.3.2 QFP and Chip Resistor Lead Intermetallic Measurements

After determining the failure location for the chip resistors, the intermetallic layer on the component lead was measured for both QFP and chip resistors. The non-linear shape of the QFP did not lend itself to a similar measurement procedure as the interfacial intermetallic layer measurement. Instead, the maximum, minimum, and visual average locations were measured. Measurements were made before and after thermal/vibration cycling, the aged data will be presented since the post cycling components feature cracking and measurement difficulties. The results of the QFP leads formed a Cu_6Sn_5 intermetallic layer the measurements aged at 185°C are summarized in Figure 32.

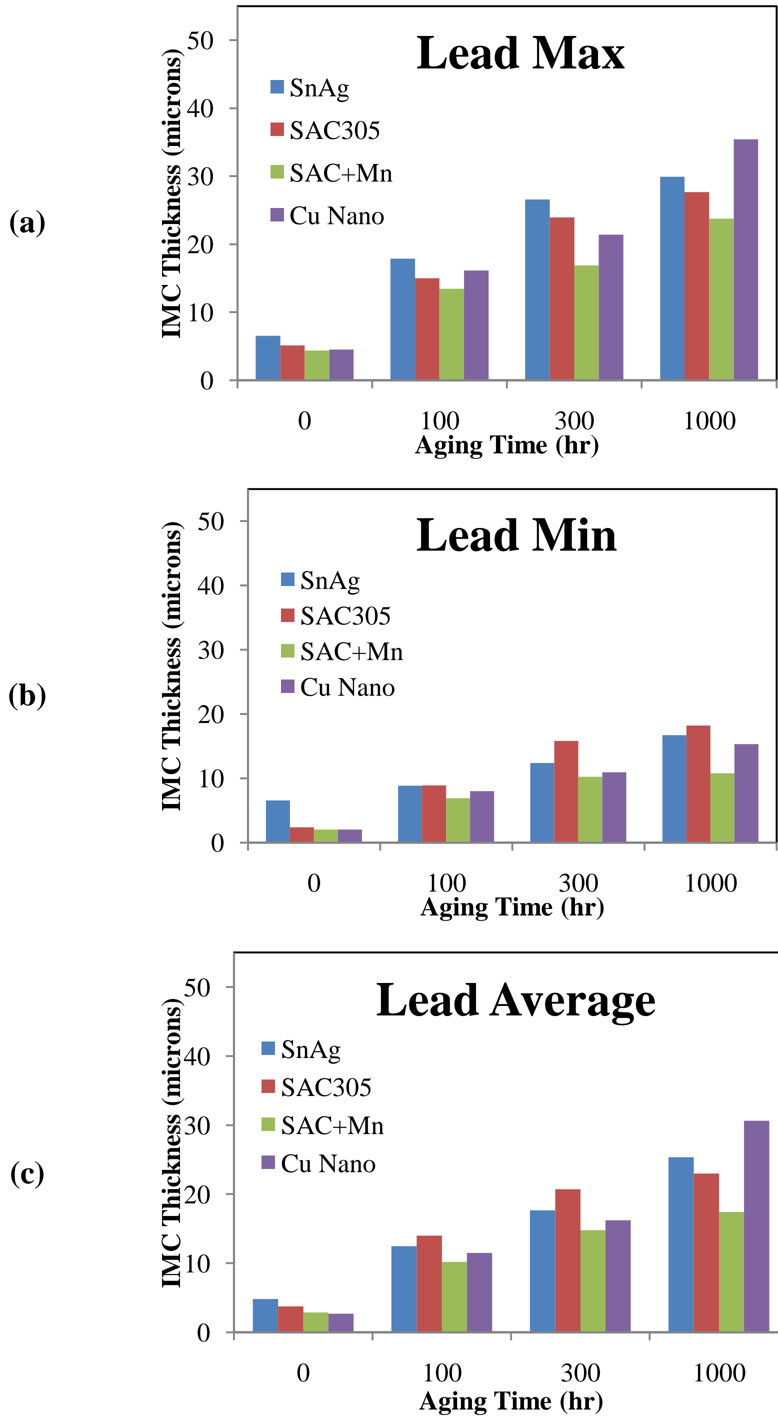


Figure 32: 185°C Aging QFP Lead intermetallic layer measurements, (a) lead maximum thickness, (b) lead minimum thickness, (c) lead average thickness.

These results are similar to the results of the interfacial intermetallic layer thickness. The SnAg+Cu Nano is effective until long aging, and the SAC+Mn suppresses the formation of intermetallic compounds the best. It is noteworthy to point out that SnAg tends for

form thicker intermetallics at the lead than SAC305. A similar assessment was made using the QFP samples aged at 200°C summarized in Figure 33.

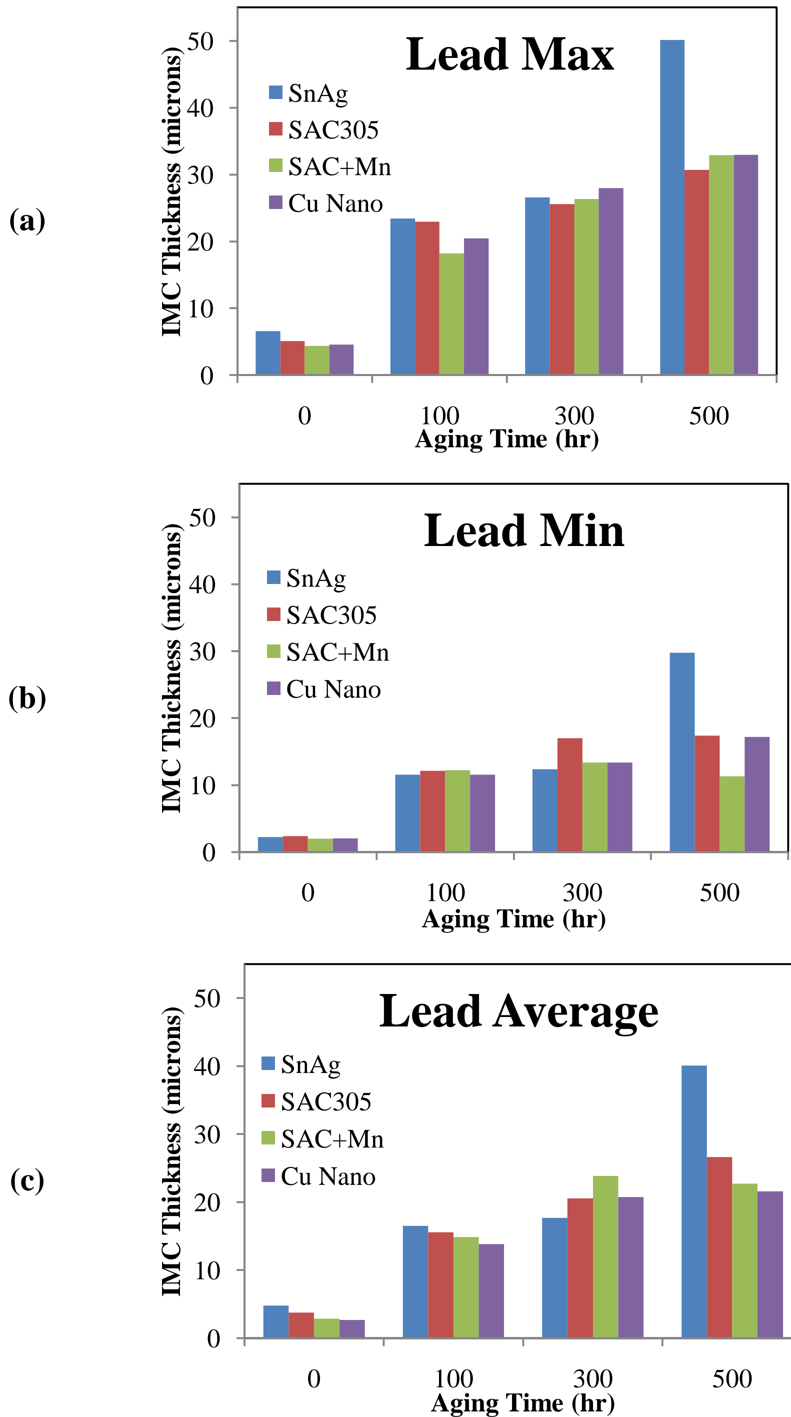


Figure 33: 200°C Aging QFP Lead intermetallic layer measurements, (a) lead maximum thickness, (b) lead minimum thickness, (c) lead average thickness.

The results of the QFP lead measurements at 200°C are similar the results from 185°C and they add a more complete picture to the interfacial intermetallic layer thickness data. At the lead side SnAg grows an extremely thick intermetallic layer. This layer suppresses the diffusion of copper into the solder bulk and limits the interfacial layer growth. Additionally, the addition of copper nano particles appears to be more effective at 200°C when viewing the lead intermetallic layer formation than only the interfacial intermetallic layer. SAC+Mn suppress the lead intermetallic layer growth similar to the interfacial results.

The chip resistors lead intermetallics were measured only for the samples aged at 200°C. The results of the measurements are summarized in Figure 34. The results of the chip resistor termination intermetallic layer thickness results are more difficult to understand and explain. There is little differentiation between the SnAg, SAC305, and SnAg+Cu nano termination intermetallic layer thickness. However, SAC+Mn rapidly grow an intermetallic layer on the chip resistor leads. This is in stark contrast with the results of the interfacial intermetallic layer growth that grows on nickel plated copper. It is believed that the presence of manganese suppresses the growth of $(Cu,Ni)_6Sn_5$ featured at the ENIG plated copper pad interface, but does not suppress the growth of $(Ni,Cu)_3Sn_4$ which grows on the chip resistor terminations. Further research is required to verify this conclusion. The growth of the thick intermetallic layer is believed to be responsible for the poor durability data of the SAC+Mn. Other explanations for these results will be examined as well, but the thick intermetallic layer on the resistor terminations poses a serious threat to reliability of the solder joint.

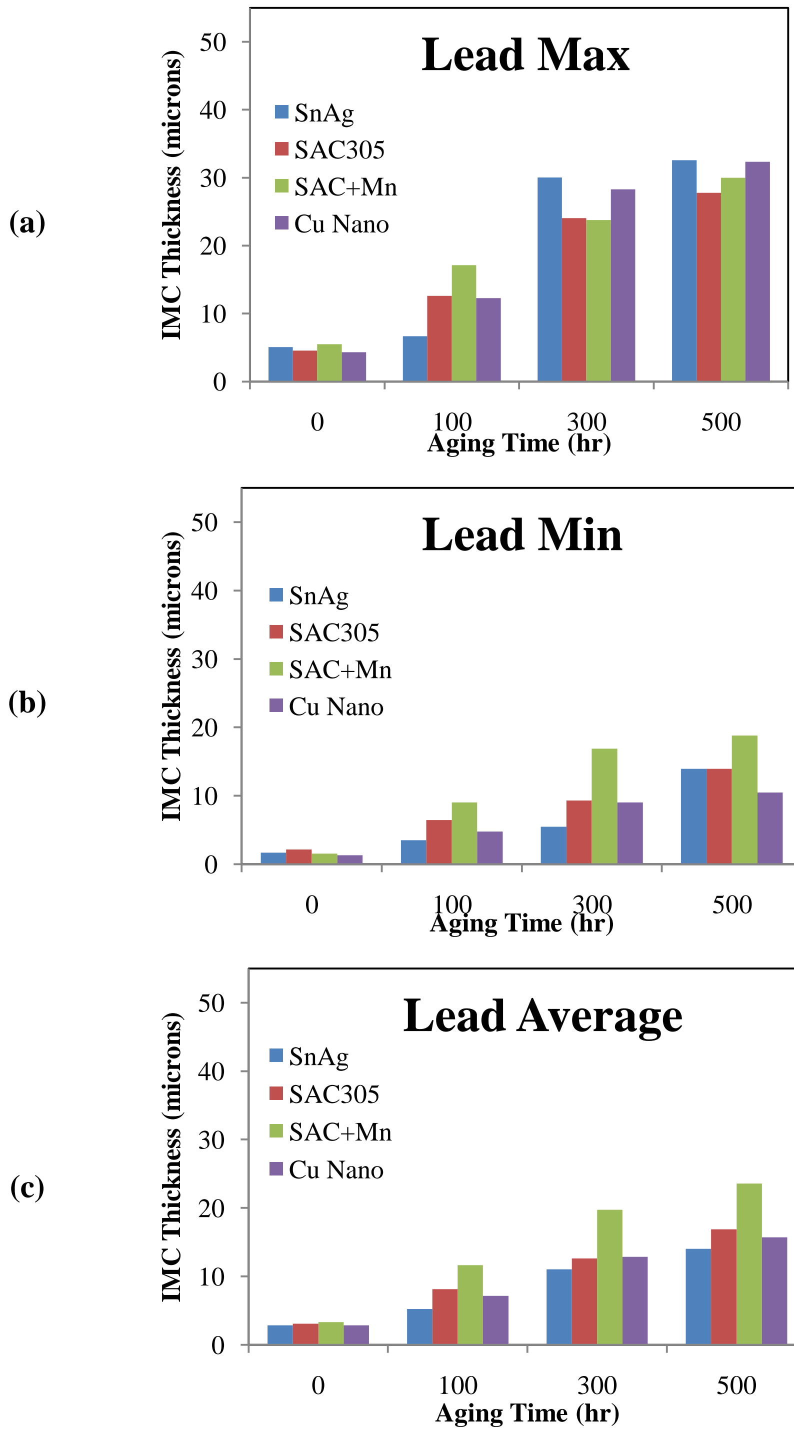


Figure 34: 200°C Aging 2512 chip resistor termination intermetallic layer measurements, (a) lead maximum thickness, (b) lead minimum thickness, (c) lead average thickness.

6.3.3 Solder Joint Quality Assessment

Finally, the SAC+Mn and SnAg+Cu Nano solder joints were assessed for other possible explanations of early failures. SAC+Mn solder joints tend to suffer from inadequate solder volume. Examples of subpar quality joints are shown Figure 35.

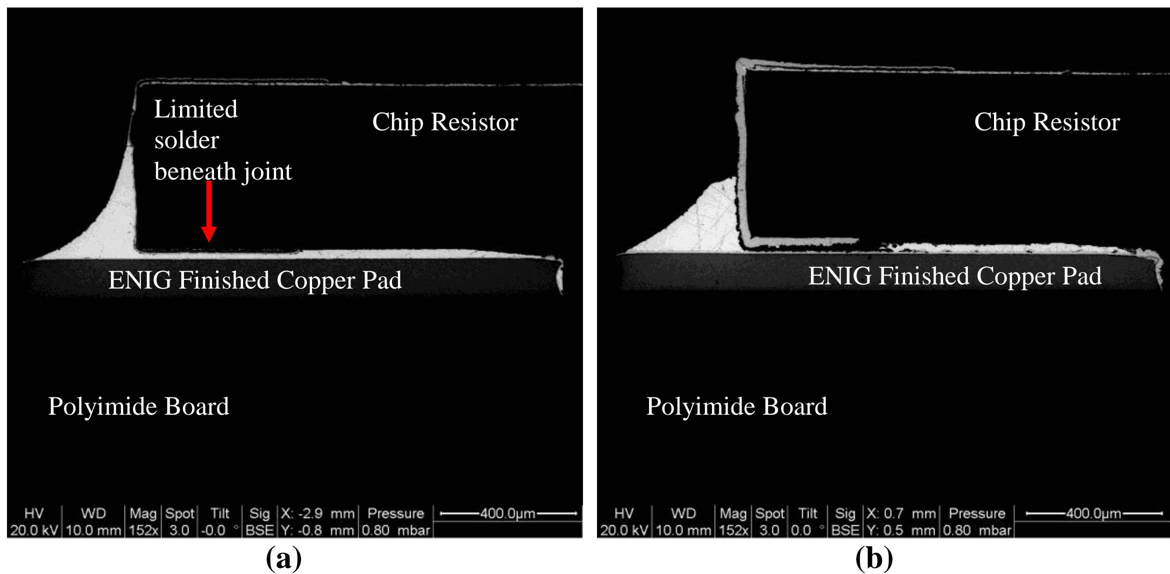


Figure 35: Examples of poor manufacturing of SAC+Mn chip resistor joints, (a) as reflowed (b) 500hr aging at 200°C (courtesy CALCE).

In Figure 35a, the SAC+Mn solder joint is shown after reflow. There is limited solder underneath the resistor which quickly transforms into thicker intermetallic layers as shown previously in Figure 34. In Figure 35b, after 500 hours of aging, the SAC+Mn fillet is very small and no solder exists underneath the resistor lead. Without any durability testing this joint has already cracked. The limited solder combined with the increased growth of intermetallics on the resistor leads is believed to be the reason for the poor durability of the SAC+Mn solder despite the suppression of intermetallic formation at the ENIG plated copper interface.

SnAg+Cu Nano joints suffer from a different manufacturing defect. The addition of copper nano particles tends to create large voids in the solder joints. As noted in Chapter 5, more prevalent voiding was viewed during the aging study. Additionally, during the failure analysis voids were noticed near cracked interfaces which are expected to initiate more easily. In Figure 36, two examples of extreme voiding are shown.

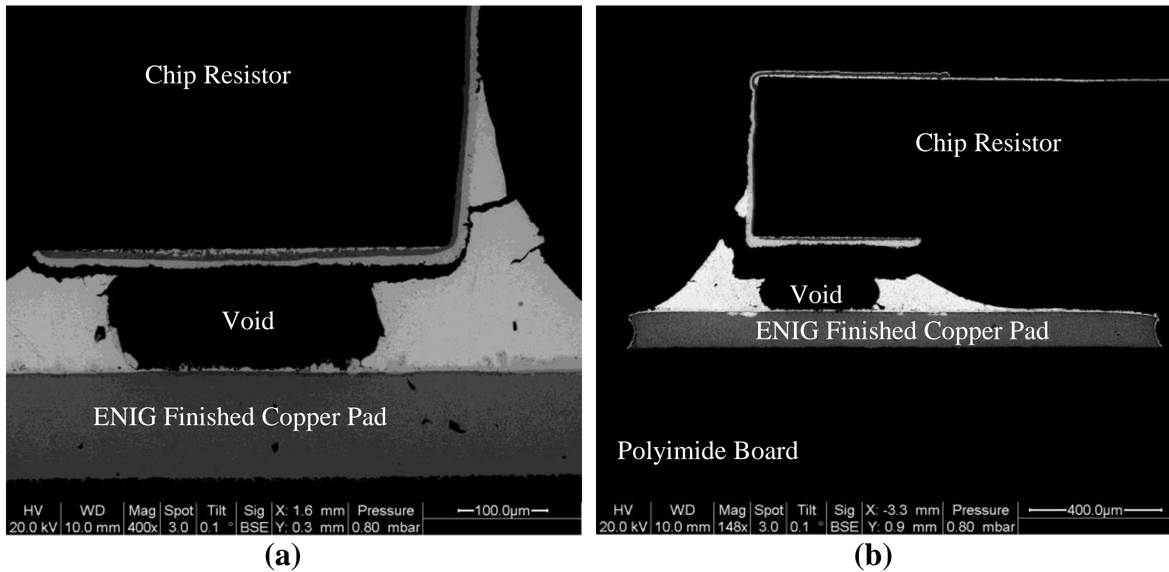


Figure 36: Examples of SnAg+Cu Nano chip resistor joint voiding observed during failure analysis, (a) 100hr aging at 200°C, (d) 500hr aging at 200°C (courtesy CALCE).

Several possible explanations for voiding in the copper nano particle solder. First, the nano particles have a thin oxidation layer which may affect the solder joint formation. A stronger flux could be used to dissolve this layer and possibly eliminate this problem. Currently, the copper nano particles were mixed into SnAg solder paste that featured RMA390 flux. Potentially, this flux is reacting poorly with the copper oxide creating larger voids. Finally, the copper nano particle shape and dispersion could negatively affect the solder joint formation. Further study to deduce the true explanation of the increased voiding found in the SnAg+Cu Nano particle solder joints is required.

6.4 Discussion of Durability Testing Results

Several interesting results were obtained from the durability testing. SAC305 outperforms the other commercial solder choice SnAg when subjected to extreme temperature cycling and vibration cycling. The literature review pointed to SAC405 performing better in high temperature cycling alone. However, further study indicated the high silver content would be detrimental to vibration resistance due to the formation of large Ag_3Sn needles and platelets. SAC305, 3.0 wt% silver, outperforming eutectic SnAg, 3.5 wt% silver, indicates that 3.0 wt% silver is a compromise between shock and vibration resistance with improved thermal cycling performance.

Additionally, the research solder alloys, SAC+Mn and SnAg+Cu Nano, did not show improved durability as expected. The isothermal aging study indicated the solder joint performance should increase as a result of the suppression of the interfacial intermetallic layer formation. The manganese dopant suffers from an increase of the growth of $(Ni,Cu)_3Sn_4$ on the resistor leads that consumes all the solder beneath the termination reducing the wetted solder joint surface area. However, the manganese dopant suppresses the interfacial intermetallic layer at higher temperatures for extended duration and the growth of copper based intermetallics. The copper nano particle addition did not show good durability either, which is believed to be a result of the excessive voiding. Further study should focus on solving the manufacturing issues associated with the novel solder alloys and understanding the impact of manganese on $(Ni,Cu)_3Sn_4$ intermetallic growth.

Chapter 7: Shear Strength Test and Correlation to Reliability

Shear testing of the 2512 chip resistors was performed according to the procedure described in Chapter 4. After shearing, samples were saved for analysis to determine the fracture location.

7.1 185°C Shear Testing Results

Three resistors were sheared after each aging condition and after each interval during the reliability testing protocol. Trends regarding shear strength versus aging time and shear strength versus thermal/vibration cycling will be discussed.

7.1.1 Shear Strength vs. Aging Time at 185°C

The strength is measured in kilograms of force, the output of the Dage2400 rather than in terms of stress because the geometry of the solder joints changes between solder to solder and joint to joint. Shear yield strength indicates the material properties whereas the force to cause failure indicates the joint quality varies.

The results of the shear strength measurements versus isothermal aging time at 185°C are shown in Figure 37. Shear strength reduction is not exacerbated until after the 300 hour aging condition. The SnAg+Cu Nano joints are initially stronger than the other solder joints. The addition of copper nano particles into the bulk solder act as a material strengthener [47]. However, after long aging, 1000 hours, the solder becomes the weakest. This corresponds with the interfacial intermetallic layer thickness. Long aging appears to reduce the effect of the nano particle addition, with the nano particles reacting to form intermetallics, thus also reducing the strengthening effect. The initial SAC305

measurement appears to be lower than expected. After aging 100 and 300 hours the data indicates the joints are stronger.

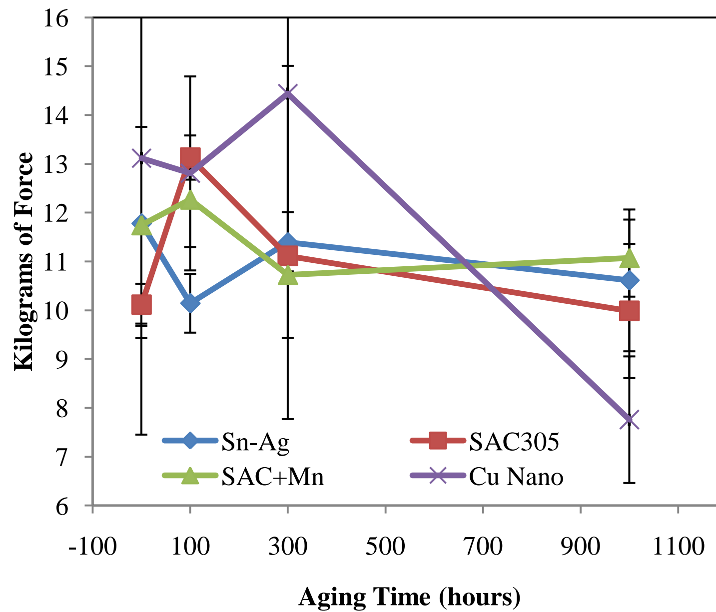


Figure 37: Shear Strength versus aging time at 185°C.

Overall, this data does not indicate that isothermal aging has a large impact on the overall shear strength of the solder joints when aged at 185°C especially for less than 1000 hours.

7.1.2 Shear Strength versus Thermal/Vibration Cycling

The damage caused by the thermal and vibration cycling has a larger impact on the strength of the solder joints than the isothermal aging condition. In general, a significant reduction is shear strength is found after the first interval of thermal and vibration cycling. The results of the impact of thermal/vibration cycling intervals for each solder is displayed in Figure 38 for each isothermal aging condition.

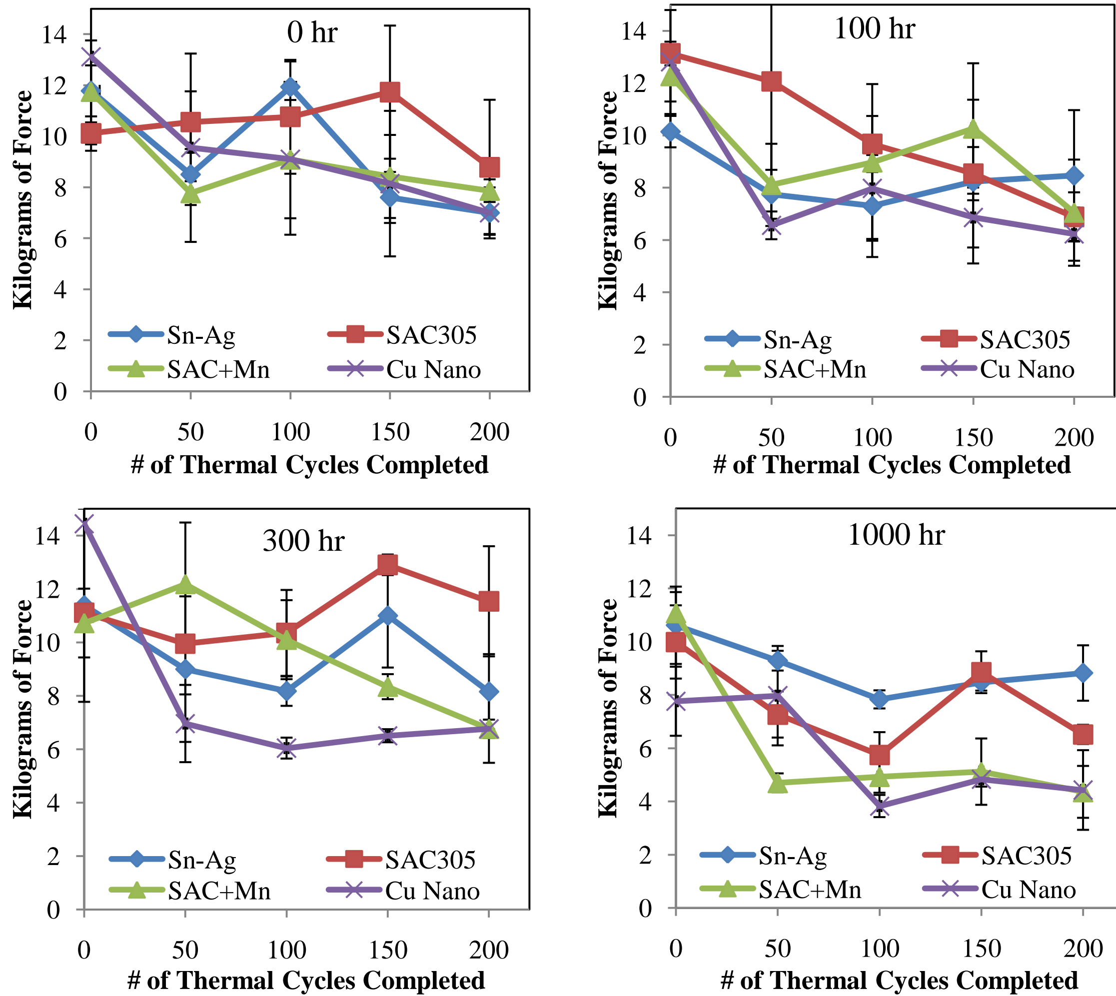


Figure 38: Shear Results by aging time 185°C, comparing shear strength versus thermal/vibration cycles completed, at each interval of 50 thermal cycles vibration cycling was performed.

SAC+Mn and SnAg+Cu Nano show the least strength as a result of the joint mechanical stressing. SAC305 and SnAg experience a less dramatic reduction in strength compared to the novel solders tested. Interestingly, the SAC305 and SnAg samples aged for 300 hours outperform the samples aged for 100 hours. Rodekohr et al. discussed a trend that increasing the thickness of the Cu_3Sn intermetallic layer will strengthen the solder joint despite increasing overall thickness [21]. This effect is believed to cause the increased strength of the SAC305 and SnAg solder joints aged for 300 hours. After 1000 hours, the shear strength does not exhibit the same trend indicating this mechanism of strengthening

is only temporary. There appears to be a trend between reduction in shear strength and risk for failure. However, with the limited sample size of the data from this study, a trend can only be observed. Further shear study with a larger shear sample size could attempt to correlate shear strength and the risk of failures.

7.2 200°C Shear Testing Results

In this test, only two 2512 chip resistors were sheared for each solder for every testing interval. The trends regarding shear strength versus aging time and shear strength versus thermal/vibration cycling will be discussed in a similar manner as the results from the 185°C test.

7.2.1 Shear Strength vs. Aging Time at 200°C

The 200°C aged chip resistors shear strength shows a greater relationship between isothermal aging and shear strength than the 185°C aged chip resistor shear results. In Figure 39, the results of the shear strength as a function of isothermal aging at 200°C are shown. Significant weakening of the solder joints can be seen after only 100 hours of aging for all solders. After 300 hours of aging, every solder is far weaker than after reflow.

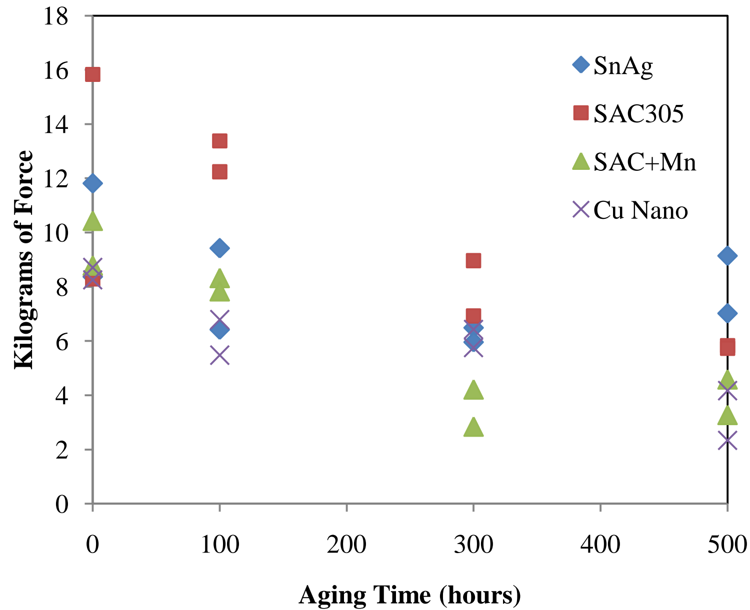


Figure 39: Shear Strength versus aging time at 200°C.

SAC305, SAC+Mn, and SnAg+Cu Nano show over a 60% reduction in shear strength after 500 hours of aging compared to the initial as reflowed condition. SnAg does not experience as dramatic of a reduction in shear strength, however the reflowed condition compared to the minimum shear strength value is approximately a 50% decrease in strength. Isothermal aging at 200°C has a more significant effect on the solder joint shear strength.

7.2.2 Shear Strength versus Thermal/Vibration Cycling

Figure 40 shows the results of the 200°C test shear testing. Isothermal aging has a larger impact on shear strength, making it harder to see the influence of the thermal/vibration cycling on solder joints that have already been weakened by isothermal aging. Thermal/vibration cycling decreases shear strength after isothermal aging until the joint is below a threshold strength value ~7-8 kilograms of force. Below this value, the shear strength is fairly level.

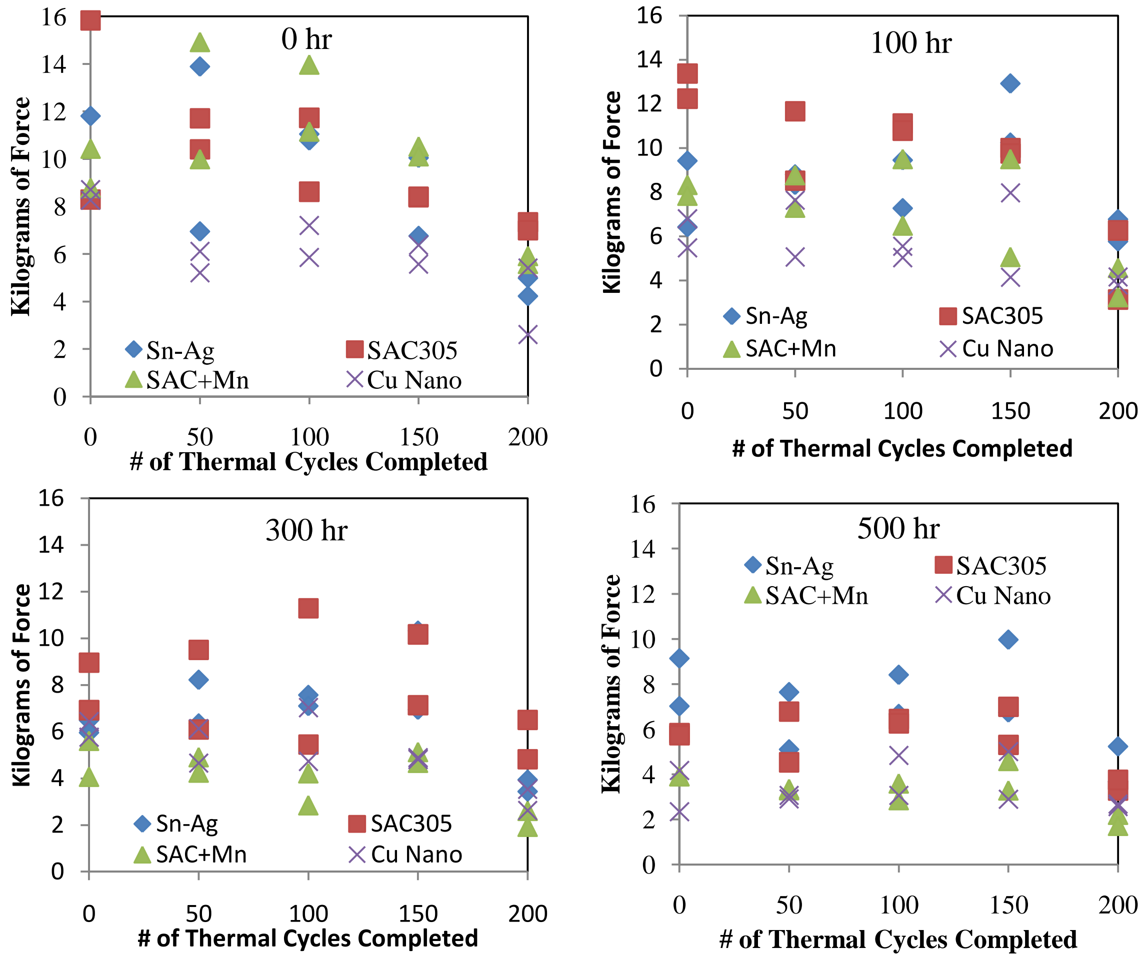


Figure 40: Shear Results by aging time at 200°C, comparing shear strength versus thermal/vibration cycles completed, at each interval of 50 thermal cycles vibration cycling was performed.

After 300 hours of aging at 200°C, all the solders are severely weakened as shown in the aging comparison. The shear strength after 300 hours of aging remains relatively constant during thermal and vibration cycling, indicating further mechanical damage is no longer affecting the solder joint shear strength.

7.3 Fractography Analysis

After chip resistors were sheared, the chip resistor and test boards were saved in order to analyze the fracture location. Based on the parameters chosen for the shear testing, failures in the intermetallic layers and intermetallic layer interfaces were desired.

Fractures in the locations mentioned would replicated the failure locations found during reliability testing, indicating a potential correlation between shear strength and the risk of solder joint failure.

7.3.1 Fracture Location

Utilizing the EDS system, the composition of the fracture surfaces were used to identify the fracture surface, and thereby the fracture location. Shear testing induces failures at two locations. The first failure location is the interface between the nickel intermetallics growing on the chip resistor lead and the bulk solder. The other failure site is between the chip ceramic body and nickel lead/nickel intermetallic chip termination. Failures were expected at these interfaces due to the rapid shear rate used to replicate stress conditions during reliability testing. Figure 41 shows an example of both failure locations.

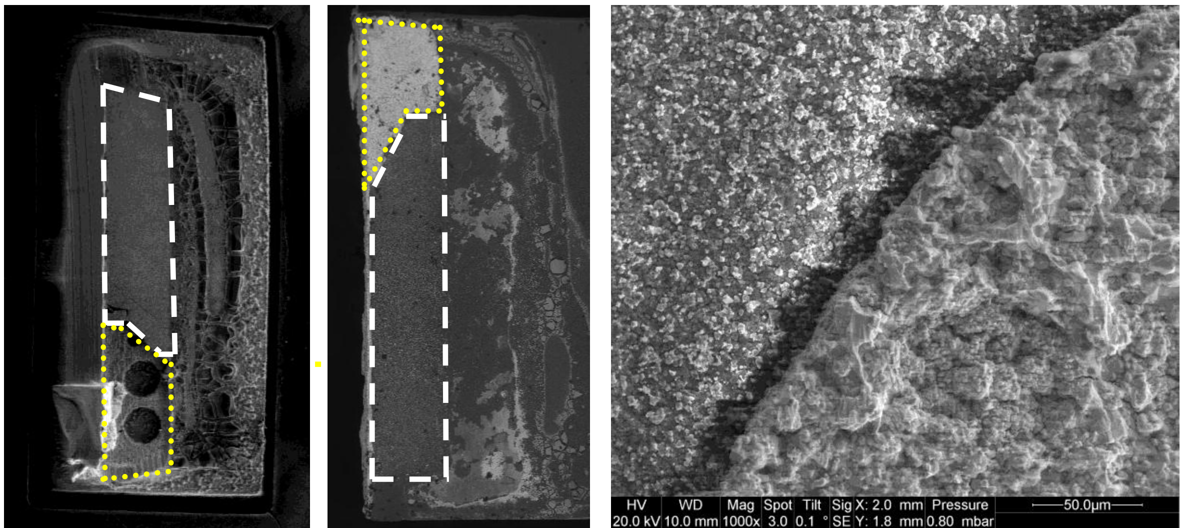


Figure 41: SAC305 500 hour aging 0 thermal/vibration cycles, left, solder joint on board, middle, corresponding chip lead flipped across horizontal axis, right, zoomed in fracture surface on chip lead (courtesy CALCE).

All three images in Figure 41 are images of the one SAC305 joint that was isothermally aged for 500 hours at 200°C with zero thermal and vibration cycles. Both failure locations agree with the failures viewed after the thermal and vibration cycling. In the

example above, about one third of the joint fractured between the solder bulk and the nickel intermetallic layer on the chip lead and the other two thirds fractured between the chip ceramic and chip termination. In the left image, the remaining solder pad is displayed. The dashed outline represents a failure between the nickel/nickel intermetallic layer and the chip ceramic. The dotted outlined is a failure between the bulk solder and the chip termination intermetallic layer. The middle image is of the chip resistor lead that has been flipped with respect to the horizontal axis. The outlined style corresponds to the same layers as the image to the left. The right image in Figure 41 displays the change in fracture surface located on the chip lead at 1000x in which the height difference between failure locations is apparent. This result shows that the shear study replicated both the failure type.

7.3.2 Voiding Discussion

In addition to determining the failure locations of shear testing, information about the solder joints was also determined. Nearly every joint that failed at the bulk solder/chip intermetallic layer revealed large voids in the solder joint. It is believed that large voids in the bulk solder led to the failure site at the bulk solder/chip intermetallic layer interface. This was not exclusive to the novel solders; however the SnAg+Cu Nano exhibited the most dramatic voiding. In Figure 42, three solder joints are shown post shear testing at 54x magnification, with the approximated soldered surface outlined by the dashed lines. All three joints have continuous failures between the bulk solder and the chip intermetallic layer and display considerable voiding. Future study could utilize shear testing to assess joint quality after reflow and during testing. Void growth during aging and mechanical stressing will become present during shear testing as shown in this study.

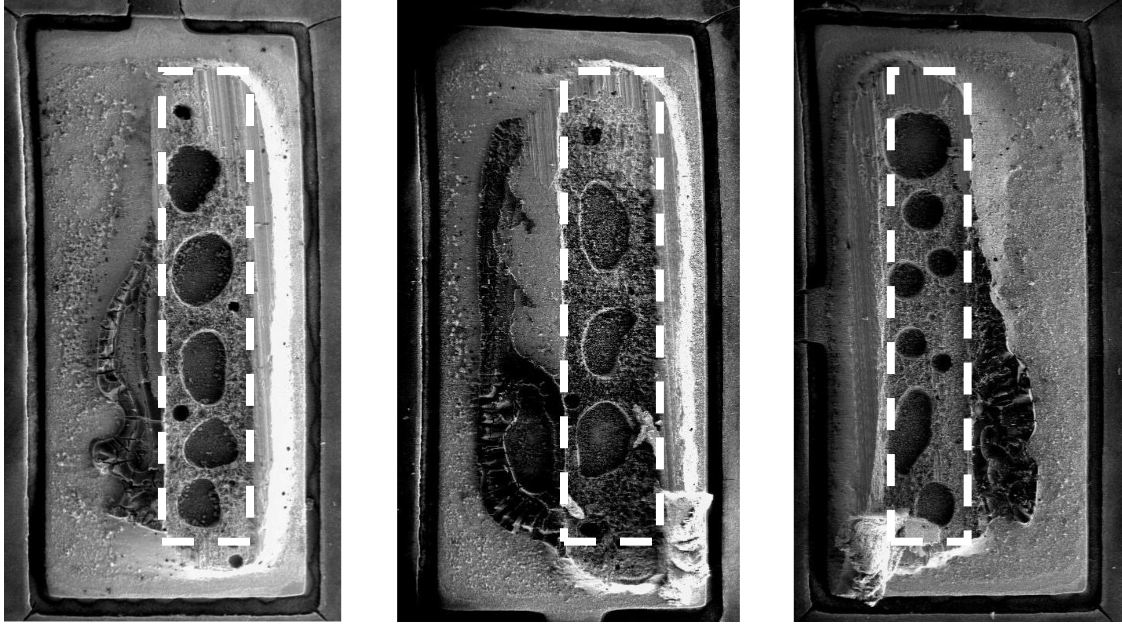


Figure 42: SnAg+Cu Nano solder joints aged 500 hours at 200°C, three shear fracture surface examples located in the remaining solder joint on the board level (courtesy CALCE).

7.4 Discussion of Shear Strength Results

Several important conclusions can be discovered from the results of shear testing. First, the isothermal aging temperature can potentially weaken the solder joints without any thermo-mechanical stressing. The fracture locations induced by shear testing match the failure locations during reliability testing indicating a correlation between shear strength and time to failure could exist. A larger sample size of shear strength samples and reliability samples is required to prove shear strength as an early indicator of failure. If this correlation is determined, it would be particularly useful for rapid testing to assess more solder and finish combinations without devoting resources to a full reliability assessment. Finally, shear fracture locations tend to indicate significant voiding. Using this information, the process control of novel solders can be rapidly assessed in order to optimize the reflow process in addition to X-ray imaging.

Chapter 8: Conclusions and Contributions

8.1 Summary of Results

The research presented in this thesis lends itself to several interesting conclusions from each of the three tests conducted. The aging study revealed the manganese dopant retarded the growth of interfacial intermetallics for both copper and nickel component leads at the PCB level. The SnAg+Cu Nano featured partial success at suppressing interfacial intermetallic layer growth. The copper leaded QFPs at 185°C and nickel leaded chip resistors at 200°C experienced a reduction in the interfacial intermetallic layer growth however, the QFP results aged at 200°C indicated the copper nano particles do not limit the interfacial intermetallic layer growth. The high temperature and availability of copper appear to be the cause of the reduced performance of the copper nano particle addition. SAC305 tended to growth thicker intermetallic layers with more variation than SnAg after extended aging at both temperatures. SAC305 formed scallops in the layers causing high variation in thickness. The SnAg and SAC305 chip resistor samples revealed an interesting phenomenon, as the nickel layer is consumed it crystallizes into a Ni-P reaction layer. This layer then transforms into a Ni-P-Sn intermetallic layer that no longer serves as a diffusion barrier to the copper pad. Copper intermetallic layers both Cu_3Sn and Cu_6Sn_5 grow beneath the Ni-P-Sn layer, consuming copper in the process. This forms four distinct intermetallic layers at the copper pad interface. This effect dramatically increases the interfacial intermetallic layer thickness.

The durability test results contradicted the hypothesis that a suppression of the interfacial intermetallic layer will increase joint reliability, requiring thorough failure analysis to better understand the results. SAC305 outperformed SnAg, SAC+Mn, and SnAg+Cu

Nano from reliability stand point when subjected to thermal and vibration cycling. Through failure analysis, the SnAg+Cu Nano alloy was determined to have poor results due to greater voiding fraction in the solder joint. This is believed to be caused by either a thin layer of oxidation on the copper nano particle addition, as a byproduct of the flux, or as a combination of the reaction between the copper oxide and flux. Further research is required to incorporate nano particles without negative effects to the joint quality. The failure analysis revealed two problems in the SAC+Mn. First, the manganese dopant is effective at suppressing the growth of the copper based $(Cu,Ni)_6Sn_5$ intermetallic but does not suppress the growth of $(Ni,Cu)_3Sn_4$ featured on the chip resistor terminations. This layer of intermetallics grew rapidly on the resistor terminations. Also, the rapid growth of intermetallics was shown to consume all the solder and no longer provide mechanical connection. These observations are believed to be the cause the SAC+Mn poor reliability.

Finally, the shear strength test demonstrated aging temperature can affect the solder joint strength. At 185°C, isothermal aging was less influential on the shear strength than thermal/vibration cycling. However, at 200°C isothermal aging greatly reduced the shear strength, especially after 300 hours of aging. Studying the fractures induced by shearing joints revealed that failure locations similar to the failures found during the thermal/vibration cycling. This indicates that the shear testing induces similar failures and potentially could predict reliability. Additionally, the fracture location also reveals information about solder joint quality. Excessive voiding causes the fracture to occur between the bulk solder and intermetallic layer interface. Using this information, the

manufacturing of novel solders can be quickly assessed in order to optimize the reflow process and improve joint quality.

8.2 Conclusions

Using the results and observations of this study several conclusions can be made.

- SAC+Mn effectively suppresses the growth of $(Cu,Ni)_6Sn_5$ and Cu_6Sn_5 intermetallic layers that can form at the PCB or component level at 185°C and 200°C but is ineffective suppressing the growth of $(Ni,Cu)_3Sn_4$ featured on the chip resistor terminations.
- SnAg+Cu Nano successfully suppresses intermetallic growth at 185°C but is less effective at higher temperature with sufficient copper present from component lead that dissolves into the bulk solder.
- Phosphorus, used for electroless nickel plating of ENIG surface finish, crystallizes with nickel as the nickel is consumed into interfacial intermetallics. The crystallized nickel phosphorus layer evolves into a Ni-P-Sn intermetallic layer which no longer serves as a diffusion barrier and allows for rapid growth of intermetallic layers.
- SAC305 exhibits the best durability during thermal/vibration cycling and displays the highest shear strength of the solders selected in this study.
- SAC305 and SnAg have greater shear strength and outperform SAC+Mn and SnAg+Cu Nano in thermal/vibration cycling because of manufacturing issues.

8.3 Contributions

This work added multiple contributions to the high temperature solder joint reliability field, which are as follows:

- First interfacial intermetallic compound and thickness assessment of manganese doped SAC alloy aged at 185°C and 200°C.
- First interfacial intermetallic compound and thickness assessment of copper nano particle in SnAg solder aged at 185°C and 200°C.
- First reliability comparison of the solders in this study under both thermal and mechanical stressing at temperatures above 185°C.

Appendix A: EC-12 Sun Electronics Chamber Programs

-40 to 185°C Range Profile

For IO=0,50	Creates 50 Cycles
Rate=5.75	Sets Ramp Rate of 5.75 C/min
Wait=15	Waits 15 minutes
Set=197	at 197°C
Wait=5	Waits 5 minutes
Set=-40	at -40°C
Next IO	Repeats Cycle until 50 cycles
Wait=1	Wait 1 minute
Set=25	at 25°C
End	Ends program at room temperature

-40 to 200°C Range Profile

For IO=0,50	Creates 50 Cycles
Rate=5.75	Sets Ramp Rate of 5.75C/min
Wait=15	Waits 15 minutes
Set=212	at 212°C
Wait=5	Waits 5 minutes
Set=-40	at -40°C
Next IO	Repeats Cycle until 50 cycles
Wait=1	Wait 1 minute
Set=25	at 25°C
End	Ends program at room temperature

Appendix B: Raw Failure Data

Test 1 Failures

Component Failures Test 1			
Solder	Aging	Component	# Thermal Cycles
Cu Nano	100 hr	R 3	44
SAC+Mn	100 hr	R 2	91
SAC+Mn	0 hr	R 3	121
Cu Nano	100 hr	QFP 4	126
Sn-Ag	0 hr	R 2	146
Sn-Ag	100 hr	R 3	147
Cu Nano	100 hr	R 4	151
SAC305	0 hr	R 4	168
SAC305	100 hr	R 3	189
Cu Nano	0 hr	R 1	200
SAC+Mn	1000 hr	R 3	24
SAC+Mn	1000 hr	R 1	62
Cu Nano	300 hr	R 3	80
SAC+Mn	1000 hr	R 2	94
Cu Nano	300 hr	R 2	100
SAC+Mn	300 hr	R 3	100
Cu Nano	1000 hr	QFP 4	104
Sn-Ag	300 hr	R 3	147
Sn-Ag	300 hr	R 1	150
SAC305	300 hr	R 3	150
Cu Nano	1000 hr	R 2	184
SAC305	300 hr	R 2	185
Cu Nano	1000 hr	R 3	187
SAC305	1000 hr	R 3	200
Cu Nano	300 hr	R 2	200
Cu Nano	1000 hr	R 1	200

Test 2 Failures:

Components Failures Test 2			
Solder	Aging	Compone	# Thermal Cycles
Sn-Ag	300 hr	R 3	51
Sn-Ag	0 hr	R 2	144
Sn-Ag	0 hr	R 4	134
Sn-Ag	0 hr	R 3	168
Sn-Ag	100 hr	R 4	175
Sn-Ag	300 hr	R 1	173
Sn-Ag	300 hr	R 2	154
Sn-Ag	500 hr	R 4	199
SAC305	0 hr	R 3	199
SAC305	100 hr	R 3	169
SAC305	500 hr	R 3	151
SAC+Mn	100 hr	R 3	28
SAC+Mn	300 hr	R 4	44
SAC+Mn	300 hr	R 3	9
SAC+Mn	500 hr	R 4	14
SAC+Mn	500 hr	R 3	4
SAC+Mn	300 hr	R 2	51
SAC+Mn	500 hr	R 2	54
SAC+Mn	500 hr	R 1	100
SAC+Mn	300 hr	QFP 1	100
SAC+Mn	300 hr	R 1	195
Cu Nano	500 hr	R 1	37
Cu Nano	500 hr	R 2	41
Cu Nano	100 hr	R 2	86
Cu Nano	500 hr	R 3	86
Cu Nano	0 hr	R 1	127
Cu Nano	0 hr	R 3	134
Cu Nano	300 hr	R 1	140
Cu Nano	0 hr	R 4	150
Cu Nano	500 hr	R 4	176

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