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**The Via Minimization Problem is
NP-Complete**

by

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ABSTRACT

In this paper, we analyze the computational complexity of the so-called Constrained Via Minimization problem. Given an already routed circuit, the problem is to find a minimum cardinality set of vias for which a valid layer assignment exists using only two layers. We first prove that the corresponding decision problem is NP-complete. We then show that it remains NP-complete even if one or more of the following restrictions are imposed.

- 1) The input layout must conform to a rectangular grid.
- 2) Vias are restricted to lie at junctions which existed in the input layout.
- 3) The maximum junction degree is limited to six or more.

1. Introduction

During integrated circuit fabrication, interconnections between circuit modules are formed by patterning conductive paths from one of two or more conductive layers. Because the layers are separated by a thin insulator, it is necessary to etch holes, called *vias*, through the insulator in order to electrically connect paths on different layers. Minimizing the number of these vias increases the performance of the electrical circuit and the yield of the manufacturing process and decreases the amount of area required for interconnections. In the design of printed circuit boards, copper paths are patterned on two sides of an insulating board. In order to electrically connect paths on opposite sides of the board, contact holes must be drilled through the insulator and plated with solder. Minimizing the number of contact holes, which we will henceforth refer to as vias, decreases manufacturing cost and increases the reliability of the board.

We will refer to the region of the chip or board which is available for routing as the *routing area*. We will call the interface points on the circuit modules *terminals* and the line segments which make up the conducting paths *routing segments*. We will assume that each routing segment can be assigned to one of only two layers. A *net* is a group of terminals which must be connected together electrically and a *netlist* is a set of nets. The points other than terminals where two or more routing segments meet and are electrically connected will be called *junctions*. A via is required at a junction if routing segments from two different layers are to be joined. The number of routing segments which meet at a particular junction will be referred to as the *junction degree*. A *crossing* is a point where two routing segments which are not electrically connected intersect. A layer assignment is *valid* if no two routing segments that cross are assigned to the same layer and no two routing segments that form a junction without a via are assigned to different layers.

A *routing problem* consists of a routing area, a set of modules with terminals on them, and a netlist. A *complete routing solution* consists of a set of routing segments, a set of vias, and a valid layer assignment which correctly realizes the interconnection requirements

specified by the netlist. An example is shown in Figure 1. A *partial routing solution* is a set of routing segments for which a complete routing solution exists. Throughout this paper, we will use the term “layout” rather loosely to mean any collection of routing segments and vias. We say that a layout is *grid based* if all of its routing segments are parallel to one of two perpendicular axes.

The Unconstrained Via Minimization problem(UVM) is defined as follows:

(UVM) Given a routing problem P , find a complete routing solution for P which requires the fewest number of vias.

Several authors [10,12] have obtained results for a very restricted version of this problem which places all of the terminals on the boundary of the routing area and does not allow any modules inside the routing area. Although Marek-Sadowska [12] claimed that this problem is NP-hard[†], she failed to show a convincing proof.

The Constrained Via Minimization problem(CVM) is defined as follows:

(CVM) Given a partial routing solution T for a particular routing problem P , find a complete routing solution for P which includes T and a minimum cardinality set of vias.

Unlike UVM, in CVM minimizing the number of vias is a secondary consideration since the placement of the routing segments has already been determined by some other method. This allows more important criteria such as area or path length to be given preference. It should be noted that the true minimality of a CVM solution depends somewhat on what are considered possible locations for vias. We will refer to the sites considered for vias as *via candidates*.

Hashimoto and Stevens [9] first suggested the CVM problem in 1971. Their problem was thought to be NP-hard for nearly a decade, leading other researchers to develop heuristic algorithms [16] or use integer programming with branch and bound techniques to obtain an optimum solution [4]. In 1980, Kajitani [11] showed that the problem can be solved in polynomial time when the layout is restricted to be grid based and all nets

[†] See [8] for complete definitions of NP-completeness and NP-hardness.

contain exactly two terminals. This encouraged other researchers to look for a polynomial time solution for the more general case. In 1982, Pinter [15] obtained optimum results for the case when the maximum junction degree is limited to three, but his algorithm can not be applied to layouts which contain junctions with higher degree.

It should be noted that in the general case, a layout may contain junctions of any degree, but in the case of grid based layouts only eight wires can be joined at a single point. However, in order to obtain a more globally optimum solution for a grid based layout, it is desirable to merge adjacent junctions into a special type of junction, called a *via candidate zone*, as explained in [2]. Since these via candidate zones can have arbitrarily large degree, it is important to develop algorithms which do not place restrictions on the maximum junction degree.

In 1983, Chen, Kajitani, and Chan [2] presented a polynomial time algorithm for grid based layouts which gives optimum results when the maximum junction degree is limited to three and approximate results otherwise. However, they restrict vias to lie at junctions which existed in the original layout. This precludes the placement of a via on any straight line segment where one did not exist before and thus limits the optimality of their result. Recently, Chang and Du [1] developed a heuristic algorithm which can handle junctions of any degree, but which does not guarantee optimum results for any case. More recently, Naclerio, Masuda, and Nakajima [14] developed an algorithm which has the same time complexity as Chen, et al. [2], but does not require that the layout be grid based or restrict the location of vias. Their algorithm also yields optimum results when the maximum junction degree is limited to three and good results for any other case.

In this paper, we will show for the first time that without restrictions on the maximum junction degree, the Constrained Via Minimization problem is NP-hard. For clarity, we begin by showing a polynomial transformation from the NP-complete Planar Vertex Cover problem [7] to the general CVM problem described in Naclerio, et al. [14]. We then refine our method to show a transformation from a restricted version of the Planar Vertex Cover problem [6] to the restricted version of CVM described in Chen, et al. [2].

In this manner we prove that CVM is NP-hard even when one or more of the following restrictions are made.

- 1) The input layout must be grid based.
- 2) Only junctions in the input layout are considered via candidates.
- 3) The maximum junction degree is limited to six or more.

This leaves open only the cases when the maximum junction degree is limited to four or five for the problems described in [14] and [2].

2. The General CVM Problem

Let us begin by considering the general CVM problem. In this case, the partial routing solution for a given instance is not required to be grid based and may take any form. There are no restrictions on the choice of via candidates, or on the maximum junction degree. The decision problem to be considered is defined as follows:

- (*cvm*) Given a partial routing solution T and a positive integer k , does there exist a complete routing solution which requires k or fewer vias?

Note that k may be bounded by $|T|^2$, where $|T|$ is the number of routing segments in T , since more than one via along any conductive path between any two crossings is never required. Thus, a solution with k or fewer vias could easily be guessed non-deterministically in polynomial time. Since it is easy to test if that solution is valid, we know that $cvm \in NP$. In order to show that the problem is NP-complete, we will show a polynomial transformation from the Planar Vertex Cover problem (PVC) [7] whose decision problem is defined as follows:

- (*pvc*) Given a planar graph $G = (N, E)$ and a positive integer k , does there exist a vertex cover N' for G satisfying $|N'| \leq k$?

A *vertex cover* for a graph $G = (N, E)$ is a subset $N' \subseteq N$ such that for each edge $(n_i, n_j) \in E$, $n_i \in N'$ or $n_j \in N'$. The *pvc* problem was shown to be NP-complete in Theorem 2.7 of [7].

In order to construct the transformation, we will use the sublayout H shown in Figure 2. Note that H requires at least one via if it is to be realized using only two layers. If that via is placed at either the junction labeled v_s or the junction labeled v_t , then a valid layer assignment will exist for H .

Lemma 1. *If we create a layout L by joining one or more non-overlapping sublayouts identical to H together at either v_s or v_t , and replacing either v_s or v_t from each of the H 's with a via, then L will have a valid layer assignment.*

Proof: We will define an *independent sublayout* I as a portion of a layout whose routing segments intersect routing segments not belonging to I only at vias. Because of this property, routing segments within a particular independent sublayout I can be assigned to layers without considering the layer assignment of any segments which do not belong to I . Any layout L constructed in the manner described above can be partitioned into two types of independent sublayouts which are shown in Figures 3 and 4. The independent sublayouts of Type 1 consist of a single H and have a via at both v_s and v_t . The independent sublayouts of Type 2 are made up of one or more H 's joined at a single junction j and have a via at whichever of v_s or v_t is not coincident with j . As shown in Figures 3 and 4, valid layer assignments exist for both types of independent sublayouts. Since L is made up of only two types of independent sublayouts and both types of independent sublayouts have valid layer assignments, we know that the entire layout has a valid layer assignment. ■

We are now ready to construct a polynomial transformation from *pvc* to *cvm*. Given an instance of *pvc* consisting of a planar graph $G = (N, E)$ and a positive integer k , we will generate an instance of *cvm* consisting of a partial routing solution T_G and the same integer k . Let \overline{G} be a planar embedding of the graph G such that every edge is a straight line segment and no two edges intersect, except at their endpoints. We will call such an embedding a *straight line planar embedding*. There are several well known algorithms for obtaining a planar embedding of a graph in polynomial time (for example [3]). Fary [5]

showed that any such embedding can be converted to a straight line planar embedding in polynomial time. We will form a small region around each edge (s,t) in \overline{G} in such a manner that no two regions overlap. This will always be possible since no two edges intersect in the planar embedding. Next, we will replace each edge (s,t) with a sublayout H in such a manner that H is completely within the region surrounding the edge (s,t) and that v_s and v_t coincide with s and t , respectively. We call the resulting partial routing solution T_G . Figure 5 shows a straight line embedding for a graph G_a and the partial routing solution T_{G_a} obtained from it.

Assume that G has a vertex cover N_1 such that $|N_1| \leq k$. By definition, N_1 must include at least one endpoint from each edge in E . Let V_1 be the set of vias which is made up of exactly the junctions that correspond to the vertices in N_1 . V_1 will include either v_s or v_t (or both) from every H and $|V_1| = |N_1|$. Thus, by Lemma 1, V_1 is a set of vias of size k or less for which a valid layer assignment for T_G exists.

Now assume that there is a set of vias V_2 , of size k or less, for T_G for which a valid layer assignment exists. From our discussion, we know that V_2 must include at least one via located in every H . Although there are no restrictions in *cvm* on the location of vias, we will assume that all vias are placed at junctions which originally corresponded to either v_s or v_t for some H . This does not affect the generality of the solution, since a via placed elsewhere could easily be moved to either v_s or v_t , in the same H without increasing the total number of vias or affecting the existence of a valid layer assignment. Since the sublayouts overlap only at v_s and v_t , there would be no reason to place a via elsewhere. Thus, V_2 will include at least one via placed at either v_s or v_t (or both) for each H . Let N_2 be the set of vertices which correspond to the vias in V_2 . N_2 will include at least one endpoint of every edge in E and thus constitutes a vertex cover for G with $|N_2| = |V_2| \leq k$.

Since the transformation from *pvc* on G and k to *cvm* on T_G and k described above only requires replacing each edge in the straight line planar embedding of G with the sublayout H , it can easily be accomplished in polynomial time with respect to the size of the input. Thus, we have the following theorem:

Theorem 1. *cvm* is NP-complete . ■

3. The Restricted CVM Problem

In this section, we show that the decision problem associated with the restricted version of the CVM problem described by Chen, et al. [2] with the further restriction that the maximum junction degree be limited to six is NP-complete. This result will then be extended to show that for any combination of the restrictions enumerated below, the problem remains NP-complete.

- 1) The input layout must be grid based.
- 2) Only junctions in the input layout are considered via candidates.
- 3) The maximum junction degree is limited to six or more.

We will distinguish between the various decision problems by using a single subscript to denote the maximum junction degree allowed for an instance and superscripts to denote any other restrictions imposed. Thus, we will denote the most restricted decision problem as $cvm_6^{1,2}$ which is defined as follows:

$(cvm_6^{1,2})$ Given a grid based partial routing solution T with no junction having degree exceeding six and a positive integer k , does there exist a complete routing solution such that k or fewer vias are required and they are all located at junctions which existed in T ?

By the same reasoning that was used for *cvm*, we know that $cvm_6^{1,2} \in NP$. In order to prove that it is also NP-complete, we will show a polynomial transformation from a restricted version of the Planar Vertex Cover problem which is described below.

(pvc_3) Given a planar graph $G = (N, E)$ with no vertex having degree greater than three and a positive integer k , does there exist a vertex cover N' for G satisfying $|N'| \leq k$?

pvc_3 was shown to be NP-complete in Lemma 1 of [6].

Suppose we have a planar graph $G = (N, E)$ and a positive integer k as an instance of pvc_3 . We will generate an instance of $cvm_6^{1,2}$ consisting of a partial routing solution T_G^* and the same integer k . In order to accomplish this, we will first embed the graph G on a planar rectangular grid. Tamassia [17] recently presented a polynomial time algorithm to do this which generates $O(|T|)$ straight line segments. We will denote such a planar grid embedding of G by \hat{G} . We then proceed in a manner similar to that used in the previous section using a sublayout H^* shown in Figure 6. H^* also requires at least one via if it is to have a valid layer assignment. Because H^* is topologically equivalent to H , Lemma 1 will hold for H^* . We will replace each edge (s, t) in \hat{G} with an H^* in such a manner that v_s^* and v_t^* coincide with s and t , respectively, to obtain the partial routing solution T_G^* . This is done by replacing the first vertical or horizontal segment of each edge with the portion of H^* nearest v_s^* and then adapting the remaining portion to follow the rest of the line segments which make up the edge. If the H^* 's are sufficiently narrow, then no two H^* 's will intersect except at v_s^* or v_t^* . Figure 7 shows a planar grid embedding \hat{G}_a of G_a and the corresponding partial routing solution $T_{G_a}^*$. Since no vertex in G can have degree exceeding three and the junctions v_s^* and v_t^* in H^* have degree two, no junction in T_G^* will have degree exceeding six.

Assume that G has a vertex cover N_1 such that $|N_1| \leq k$. Let V_1 be defined as the set of junctions in T_G^* which correspond to the vertices in N_1 . We can show using Lemma 1 that if the junctions in V_1 are made vias, then a complete routing solution is obtained for T_G^* which requires k or fewer vias.

Now assume that there is a set of k or fewer vias V_2 which are all located at previously existing junctions in T_G^* and for which a valid layer assignment exists. We know that V_2 must include at least one via located in every H^* . Furthermore, we can assume that all of the vias are placed at junctions corresponding to either v_s^* or v_t^* since a via placed at a junction corresponding to v_u^* in some H^* , can be moved to either v_s or v_t in the same H^* . Thus, V_2 will include at least one via placed at either v_s^* or v_t^* (or both) for each H . Let N_2 be the set of vertices which correspond to the vias in V_2 . Using the same argument as in the proof of Theorem 1, N_2 will be a vertex cover for G with k or fewer vertices.

As mentioned earlier, we can construct, in polynomial time, a planar grid embedding \hat{G} of G which has $O(|T|)$ straight line segments [17]. We then generate T_G^* by replacing each line segment with a portion of the sublayout H^* . Thus, the entire transformation can be accomplished in polynomial time and we have the following theorem:

Theorem 2. $cvm_6^{1,2}$ is NP-complete . ■

It should be noted that the proof of this theorem does not have to take advantage of restriction 2 on via location. In fact, as stated in the proof of Theorem 1, vias placed anywhere can always be moved to either v_s^* or v_t^* in any H^* without affecting the results. Thus, the NP-completeness result will hold without restriction 2 and we have:

Theorem 3. cvm_6^1 is NP-complete . ■

Because restrictions 1 and 3 affect only the class of valid instances for the cvm problem, relaxing either or both of these constraints does not affect our NP-completeness results. Thus, it follows from Theorem 2 that cvm_6^2 , $cvm_j^{1,2}$, and cvm_j^2 are all NP-complete for any j greater than six. From Theorem 3, we can also deduce that cvm_j^1 , cvm_6 , and cvm_j are also NP-complete for all j greater than six. Thus, we have our strongest theorem.

Theorem 4. *The cvm problem is NP-complete given one or more of the following restrictions:*

- 1) *The input layout must be grid based.*
- 2) *Only junctions in the input layout are considered via candidates.*
- 3) *The maximum junction degree is limited to six or more.*

4. Conclusion

In this paper, we have shown that the general Constrained Via Minimization decision problem is NP-complete. We have also shown that this result holds when the input layout

is constrained to lie on a rectangular grid and/or when vias are restricted to lie at junctions which existed in the input layout. In addition, our result holds when the maximum junction degree is limited to six or more with or without any of the other constraints listed earlier.

Recently, Naclerio, et al. [14] have obtained a polynomial time algorithm for the general CVM problem when the maximum junction degree is limited to three. This leaves open only the cases when the maximum junction degree is limited to four or five. It may also be interesting to consider the case when junction degree is not bounded and all of the terminals are constrained to lie on the closed curve which bounds the routing area. In this case, the construction we used cannot be applied and it is not known whether a polynomial time algorithm may exist. This case is of interest because it includes many of the common classes of routing problems such as channel and switchbox routing.

A natural extension of the CVM problem is to consider layouts which use more than two layers. Unfortunately, Molitor [13] has recently shown that the Constrained Via Minimization problem for l layer routing is NP-hard for all fixed $l \geq 3$ when the maximum junction degree is limited to four or more. This leaves open exactly the same cases that have known polynomial time algorithms for two layer routing.

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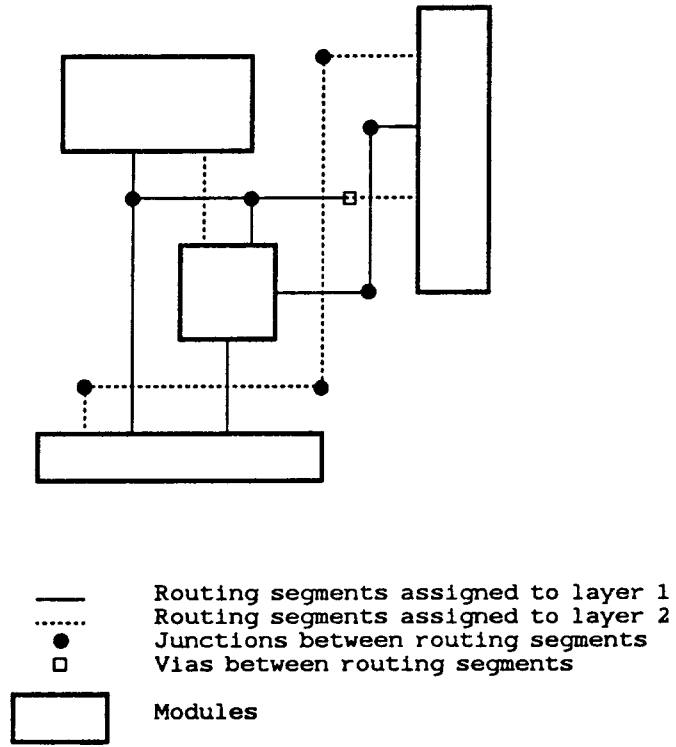


Figure 1. A complete routing solution

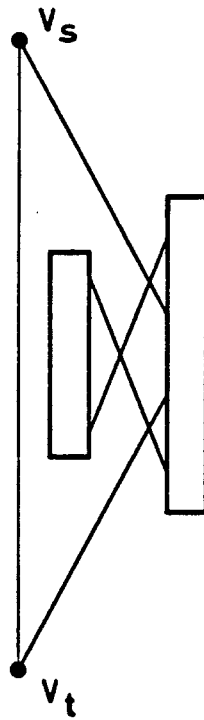


Figure 2. Sublayout *H*

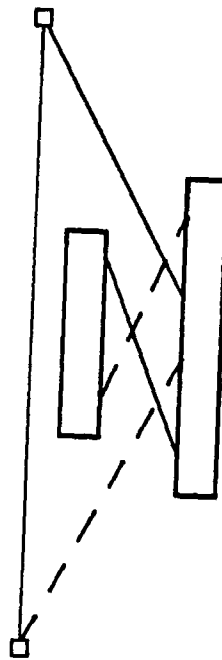


Figure 3. Type 1 independent sublayout

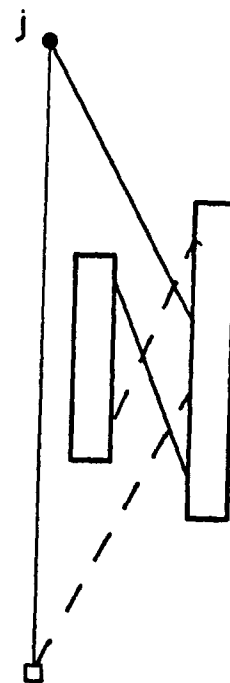
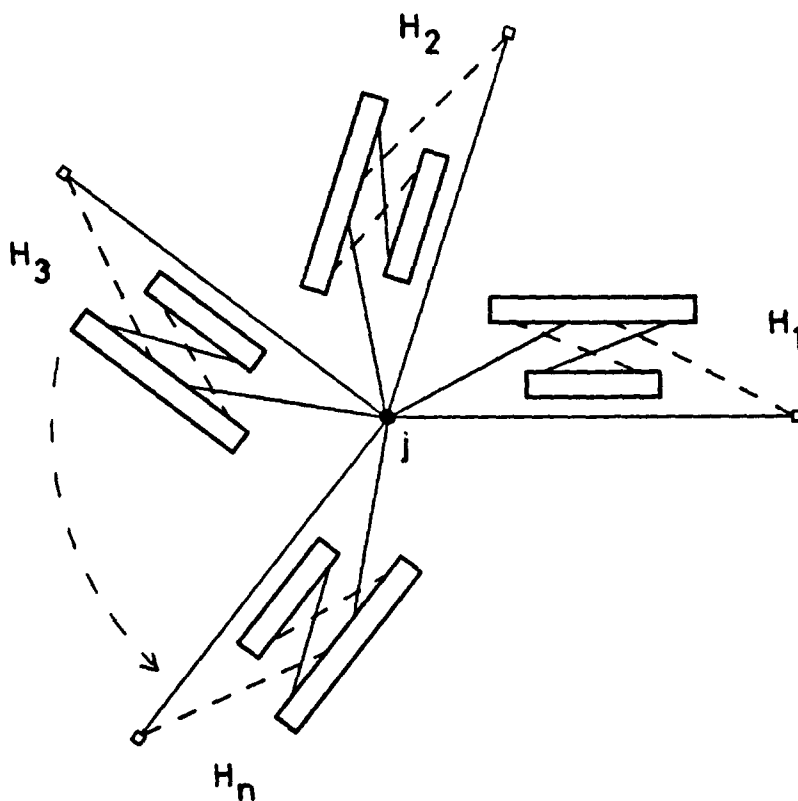


Figure 4. Type 2 independent sublayouts

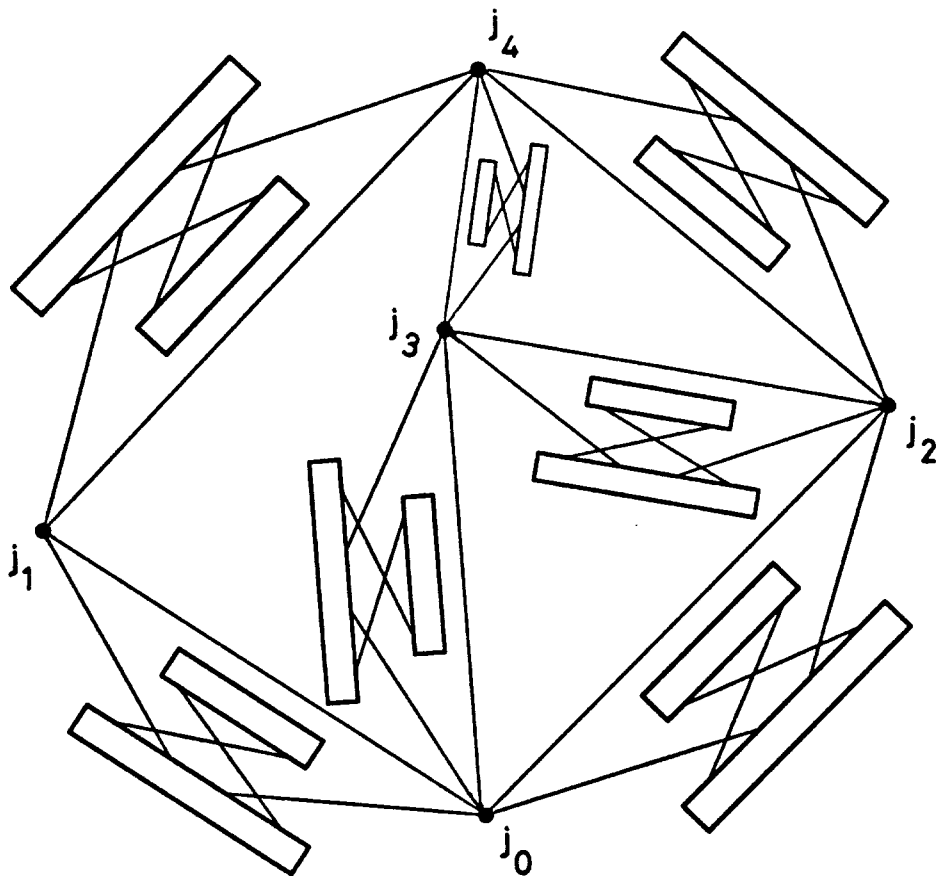
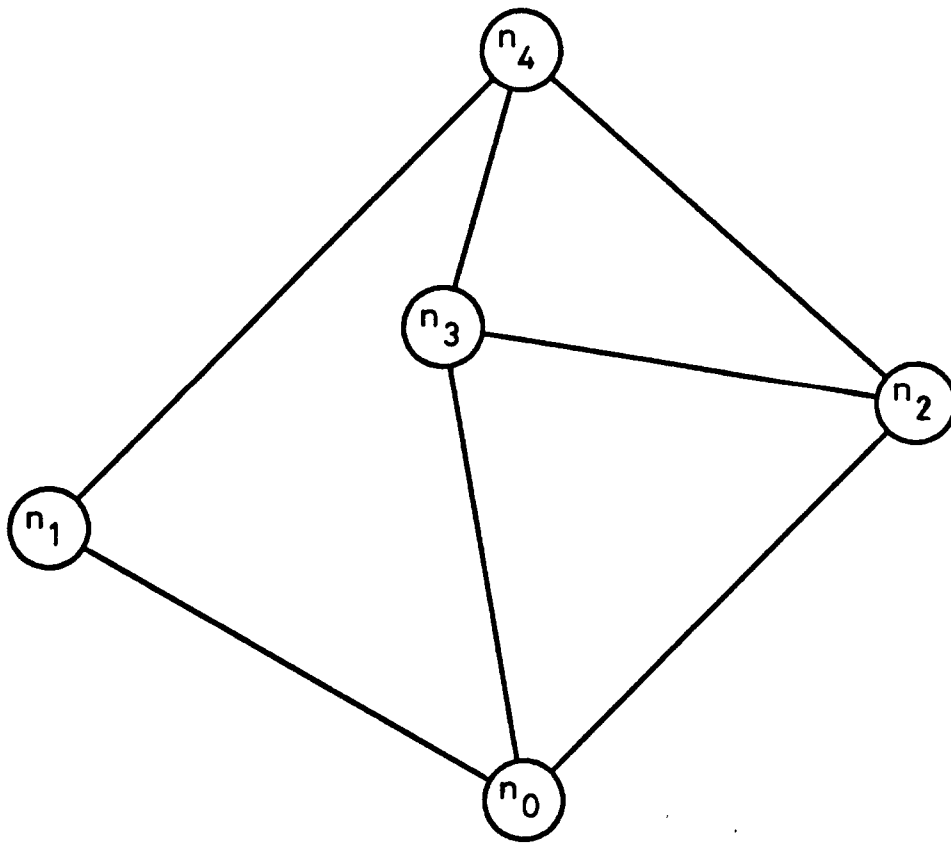


Figure 5. Straight line embedding \overline{G}_a and the partial routing solution T_{G_a} .

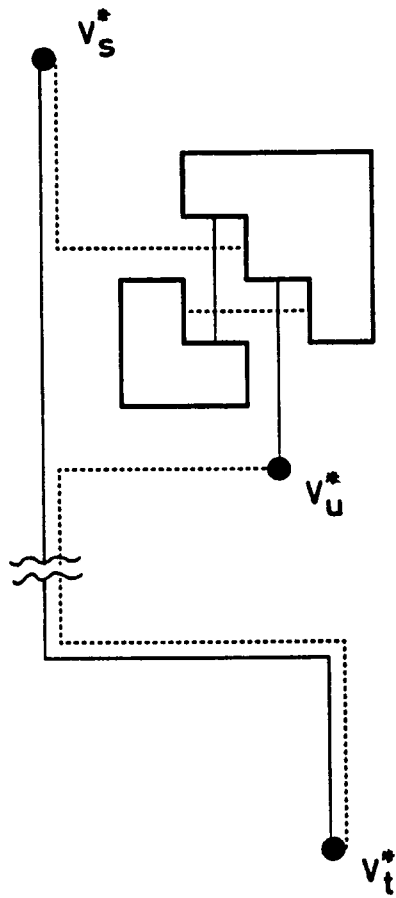


Figure 6. Sublayout H^*

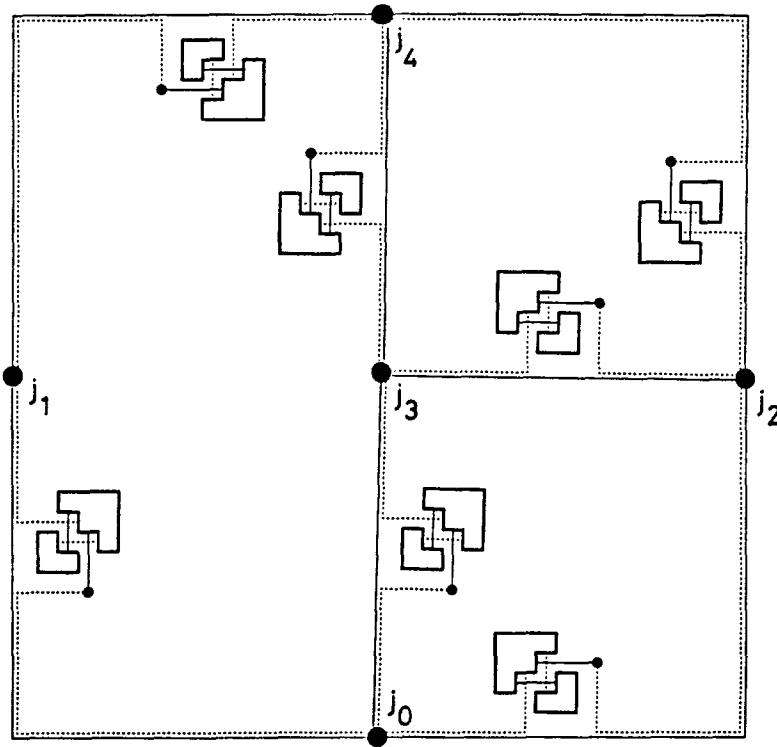
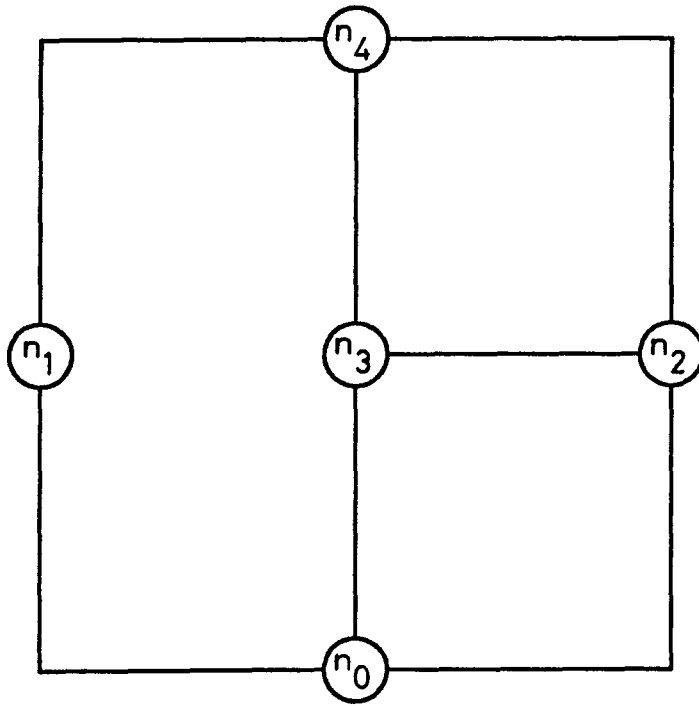


Figure 7. Planar grid embedding \hat{G}_a and the partial routing solution $T_{G_a}^*$

