ABSTRACT

Title of Thesis: PART SELECTION AND MANAGEMENT BASED ON RELIABILITY ASSESSMENT FOR DIE-LEVEL FAILURE MECHANISMS

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Electronic part manufacturers often provide reliability values in metrics such as Mean Time Between Failures (MTBF) and its inverse, Failures in Time (FIT). These metrics assume a constant failure rate and do not account for damage accumulation or wear-out phenomena, making the part selection and management based on this information meaningless.

This thesis will report on the challenges associated with manufacturers' avoidance of sharing critical part information and how insufficient information hampers decision-making for part selection. The thesis uses four die-level failure mechanisms (Electromigration, Time-Dependent Dielectric Breakdown, Hot Carrier Injection, and Negative Bias Temperature Instability) as demonstration cases. It investigates the extent to which industry-published documents can be used to obtain the data necessary to simulate these mechanisms. It will report on methods of selecting an appropriate failure model based on the part technology level and identifying the

required parameters for estimating the part's time to failure. Various scattered part information sources, literature, and industry-published documents may include the input parameters of failure models. The thesis provides insights into the complexity of understanding these information sources and various methods to obtain the required parameters to estimate the time to failure distributions.

The methodology considers the susceptibility of parts to die-level failure mechanisms and compares components for reliability. A simulation template that facilitates practical implementation by enabling designers, engineers, and procurement teams to make informed decisions while selecting electronic parts for specific applications is introduced. The research findings and methodology presented provide valuable insights for users to improve the reliability and performance of electronic systems through effective part selection.

PART SELECTION AND MANAGEMENT BASED ON RELIABILITY ASSESSMENT FOR DIE-LEVEL FAILURE MECHANISMS

By

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1. Introduction: Comprehensive Idea of Part Manufacturers Avoiding Sharing Critical Information

The practice of part manufacturers avoiding providing relevant information is a source of concern that can have significant implications for product quality, reliability, safety, and customer satisfaction [1]. The practice describes circumstances in which manufacturers intentionally withhold or give customers insufficient information, which can impede decision-making processes.

There are several reasons why part manufacturers may engage in this practice. Preserving a competitive advantage or protecting private information is one of the main drivers. Manufacturers could be reluctant to provide critical information about their manufacturing procedures, geometry dimensions, materials, or design requirements out of concern that rivals may replicate their techniques or learn information that might jeopardize their position in the market [2]. Protecting confidential information is understandable, but it becomes a problem when it prevents the customer from assessing the product thoroughly.

Part manufacturers often hesitate to provide detailed reliability information because they are often unaware of how their parts will be utilized in the end product. As a result, they may refrain from sharing specific reliability data or performance characteristics that could be useful for customers. Manufacturers typically produce parts that are used in a wide range of applications across various industries. These applications can vary significantly in terms of operating conditions, environmental factors, and stress levels. Consequently, it becomes challenging for part manufacturers to predict precisely how their parts will perform in every possible scenario. By withholding reliability information, manufacturers can avoid making claims or guarantees

about the performance of their parts in specific applications. They may fear potential liability issues if their parts fail to meet customer expectations in unforeseen circumstances or environments.

Another element that contributes to this issue is cost reduction. Gathering and providing comprehensive information takes time, effort, and resources [3]. Manufacturers may reduce these outlays by offering what is strictly necessary to comply with contracts or requirements. This approach allows them to cut costs but neglects the importance of sharing crucial details that could impact the customer's ability to evaluate the part's quality, reliability, and compatibility with their specific requirements.

Manufacturers may also refrain from disseminating helpful information due to poor communication channels and a lack of standard operating procedures. Manufacturers may undervalue the importance of giving their customers detailed data when communication is not established or there is no defined framework for information exchange. In these situations, they can presume that the client would ask for relevant information or overlook the significance of proactive information exchange [4].

The consequences of manufacturers avoiding conveying useful information can be far-reaching. Customers may face challenges understanding the part performance capabilities, potential risks, or compliance with industry standards [5]. Inadequate information can hinder their ability to make informed decisions about the part's suitability for their applications or to assess its compatibility within their existing systems or processes. This can lead to delays, additional costs, and potential safety or performance issues.

This chapter examines the part selection based on reliability assessment, which calls for manufacturer-provided information, and how the lack of information impacts the assessment.

Additionally, it offers perceptions into numerous sources of original component manufacturer (OCM) documents that only adhere to the letter of the law but do not do so in a way that effectively conveys crucial information.

1.1. Part Assessment Process

The production of a part typically involves a complex supply chain comprising various companies that are directly or indirectly involved in manufacturing constituent parts and materials for the overall part. To ensure the production of a reliable product, it is essential to carefully choose parts that possess sufficient quality and the ability to satisfy the expected performance requirements for the specified life-cycle conditions [6].

Generally, a group with considerable expertise is responsible for part selection and management. This team develops part assessment criteria and establishes acceptability levels to facilitate the selection of parts. The selection of a part is based upon its adherence to the specified requirements, its cost-effective feasibility, and its timely availability to meet the schedule requirements. In the event of any issues, the parts management team assists in identifying substitute sources of parts or devising strategies to help the supplier produce a better part. Several product design teams uphold a catalog of preferred parts with consistent reliability and performance. A "preferred part" is typically characterized by maturity and a successful manufacturing, assembly, and field operation track record.

A mature part may become undesired or obsolete because of new technologies, methods, markets, materials, and pricing pressures. A new part could be necessary when creating a brand-new product or upgrading an existing one. It is not always practicable for a client of components to dictate requirements because a company may develop parts for numerous distinct customers

with various target applications. Sometimes, it could be essential to evaluate a part beyond what the manufacturer does to choose the right one while selecting parts with the necessary qualities. Performance, quality, dependability, and ease of assembly are crucial factors in part assessment (see Figure 1) [6]. Performance is evaluated by functional assessment against the datasheet specifications. Process capability and outgoing quality metrics serve to assess quality. Results of reliability tests and part qualification are used to evaluate reliability. If a part is compatible with the machinery and procedures used in the subsequent assembly, it is acceptable from an assembly standpoint. Although all four components are necessary to complete the part assessment, we focus on the part selection based on reliability. Procurability of the part also plays vital role in performing part selection and management.

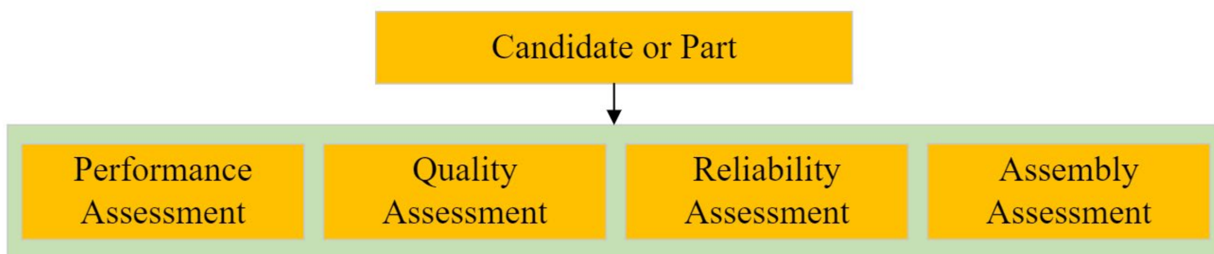


Figure 1: Part assessment process [6].

1.2. Problem with Part Reliability Information from the Manufacturer

Information regarding part qualification and reliability test results is required to perform part selection based on reliability, but obtaining part reliability information is more complex. Electronic part manufacturers usually communicate part reliability information as the mean time between failures (MTBF) or failure per billion hours (FIT). However, a constant failure rate (exponential failure distribution) as a metric reliability value does not account for the damage accumulation. Additionally, the constant failure rate estimation is based on the assumptions that

the failures during operation are random and that there is no wear-out, two rarely true assumptions for electronics [7]. Figure 2 illustrates the problem with part reliability information provided as MTBF and FIT rates. It depicts a significant change in MTBF of approximately 20,000 years depending on the confidence level for the same part and is also the same case with the FIT rates [8]. Assuming a constant failure rate, manufacturers can test a large number of parts and use the results to estimate the failure rate for a particular part number. This methodology is used because, in many cases, no failures are observed during the testing. Because of these assumptions and the lack of accounting for application conditions, it is not recommended to use failure rate data for projecting reliability metrics.

	MTBF / FIT		MTBF / FIT supporting data							
Part number	MTBF	FIT	Usage temp (°C)	Conf level (%)	Activation energy (eV)	Test temp (°C)	Test duration (hours)	Sample size	Fails	Additional comments
LM2675M-5.0/NOPB	2.9×10^{8}	3.4	55	60.0	0.7	125	1000	3388	0	-

At a 60 % confidence level
FIT Rate = 3.4
MTBF = 33,105 years

At a 90 % confidence level
FIT Rate = 8.83
MTBF = 12,922 years

Figure 2: Example of a part manufacturer reported reliability information provided as MTBF and FIT rates [8].

1.2.1. Abuse of AEC-Q100 Specifications

As the part reliability information from the manufacturer does not provide the actual reliability estimates, one can estimate the reliability of a part by utilizing the testing data performed on the part by the manufacturer. AEC-Q100 is known for failure mechanism-based stress test qualification for packaged integrated circuits (ICs) used in automotive applications [9]. The Automotive Electronics Council (AEC) established this specification to define qualification requirements and procedures for packaged ICs in the automotive industry. An AEC-Q100-

qualified device means that the device has passed the specified stress tests and guarantees a certain level of quality/reliability [10]. Automotive parts that meet the qualification requirements of AEC must complete a production part approval process (PPAP) [11] [12]. This process requires documenting the design, manufacture, and status of a part to the customer. Each PPAP document contains 18 – 20 sections, including material information, qualification testing results, and design/process failure mode effect analysis (D/PFMEA) [13]. This information is useful for comparing parts and can be used to understand the expected reliability of the part better.

According to AEC-Q100, the part manufacturer requires to complete device qualification by performing die fabrication reliability testing for electromigration (EM), time-dependent dielectric breakdown (TDDB), hot carrier injection (HCI), negative bias temperature instability (NBTI), and stress migration (SM) as shown in Figure 3. The manufacturer should provide information on sample size/lot, number of lots, acceptance criteria, and testing methods for these tests. Additionally, the data, test method, calculations, and internal criteria should be available to the user upon request for new technologies. However, it is not usual practice for many part manufacturers to provide such information.

Figure 4 represents a PPAP document from Texas Instruments for a packaged IC used in the automotive industry [14]. The first observation when Figures 3 and 4 are compared is that the manufacturer did not follow the template providing the information as per the AEC-Q100. The acceptance criteria, notes, number of lots, test method, and additional requirements columns are neglected and not included. Additionally, the naming convention is not followed in a few other columns, which can lead to confusion or improper understanding of the data. Sample size/lot is provided as SS/lot. Furthermore, new or unknown columns, such as test specification, minimum lot quantity, and duration, are included.

TEST GROUP D - DIE FABRICATION RELIABILITY TESTS								
STRESS	**ABV**	**#**	**NOTES**	**SAMPLE SIZE/LOT**	**NUMBER OF LOTS**	**ACCEPT CRITERIA**	**TEST METHOD**	**ADDITIONAL REQUIREMENTS**
Electromigration	**EM**	D1	----	----	----	----	----	The data, test method, calculations, and internal criteria should be available to the user upon request for new technologies
Time Dependent Dielectric Breakdown	**TDDB**	D2	----	----	----	----	----	The data, test method, calculations, and internal criteria should be available to the user upon request for new technologies
Hot Carrier Injection	**HCI**	D3	----	----	----	----	----	The data, test method, calculations, and internal criteria should be available to the user upon request for new technologies
Negative Bias Temperature Instability	**NBTI**	D4	----	----	----	----	----	The data, test method, calculations, and internal criteria should be available to the user upon request for new technologies
Stress Migration	**SM**	D5	----	----	----	----	----	The data, test method, calculations, and internal criteria should be available to the user upon request for new technologies

Figure 3: Die fabrication reliability tests to be performed as per AEC-Q100 [9].

Type	**#**	**Test Spec**	**Min Lot Qty**	**SS/Lot**	**Test Name / Condition**	**Duration**	**Qual Device: TPS54560BQDDAQ1**
EM	D1	JESD61	----	----	Electromigration	----	Completed Per Process Technology Requirements
TDDB	D2	JESD35	----	----	Time Dependent Dielectric Breakdown	----	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28	----	----	Hot Carrier Injection	----	Completed Per Process Technology Requirements
NBTI	D4	-	----	----	Negative Bias Temperature Instability	----	Completed Per Process Technology Requirements
EM	D5	-	----	----	Stress Migration	----	Completed Per Process Technology Requirements

Figure 4: Die reliability tests information from Texas Instruments PPAP document for part number TPS54560BQDDAQ1 [14].

The manufacturer must provide all the information, such as sample size per lot, number of lots, acceptance criteria, and testing methods for all the failure mechanisms. However, the manufacturer has not provided such information, and even the columns in the part's PPAP document were left blank. This concludes that no data related to these die-level failure

mechanisms is provided. Furthermore, it is mentioned that the device testing is performed and completed as per process technology, which depicts that the tests for these failure mechanisms are not performed for every part number but for process technology.

The PPAP provides test specifications for EM, TDDB, and HCI failure mechanisms but not for the NBTI and SM. The provided test specifications are of Joint Electron Device Engineering Council (JEDEC). JEDEC Solid State Technology Association developed the JESD61 [15]: Isothermal Electromigration Test Procedure, JESD35 [16]: Procedure for the Wafer-Level Testing of Thin Dielectrics, and JESD60 & 28 [17] [18]: A Procedure for Measuring P & N-Channel metal-oxide-semiconductor field-effect transistor (MOSFET) Hot-Carrier-Induced Degradation Under direct current (DC) Stress. The manufacturer provided these standards as test specifications for the respective failure mechanisms, and they offered the testing method. Still, the standards do not provide insights into stress application conditions, failure criteria, and the number of samples. In JESD35 [16], it is clearly stated that "the purpose of this document is to describe oxide test techniques for quick evaluation and control of oxide fabrication techniques. It does not specify acceptance or rejection criteria for any of the described procedures and, therefore, is not intended to be used to predict metal oxide semiconductor (MOS) Integrated Circuit failure rates." Based on this finding, the critical observation is that the manufacturer can toggle with the number of samples, failure criteria, and stress conditions and obtain the required qualification or reliability to satisfy AEC-Q100. With no data relevant to reliability testing, the possibility of securing part reliability through this approach is not achievable and advisable.

1.2.2. Problems with Reliability Testing

Another approach to obtaining part reliability is testing the part under usage or accelerated stress conditions to achieve time-to-failure (TTF) data on sample size. Later, these times to

failure are extrapolated to usage conditions if tested under accelerated stress conditions which are then plotted and modeled through life-stress relationships such as Arrhenius and Power-Law models to obtain the reliability of the part [19]. While testing, the number of failures depends on the testing time. Depending on the length they are tested for, there can be samples that may not fail by the end of the test, also known as censor data. While running accelerated tests, one critical aspect is extrapolating the accelerated testing data to use condition failure data for the exact failure mechanism [6]. If not, the estimated reliability could be misleading for a part reliability assessment. Even though the procedure to obtain part reliability is more accurate through this method, performing part selection based on reliability estimated through this approach is far from reach. Accelerated stress testing involves subjecting the components or products to extreme conditions for an extended period. These tests typically require significant time to observe failures and collect reliable data. In a fast-paced industry or when there are time constraints for product development and release, companies may not have the luxury of dedicating the necessary time for such tests. Accelerated stress testing can be expensive, especially involving specialized equipment, facilities, and resources. The costs associated with creating the necessary testing infrastructure, acquiring or building test setups, and conducting the tests over an extended period can be prohibitive for some companies, particularly smaller ones with limited budgets. Accelerated stress tests require skilled personnel, specialized equipment, and dedicated resources. Not all companies may have the in-house expertise or resources to design, set up, and conduct these tests.

The lack of available resources or expertise can make it challenging to perform such tests within the company. The TTF could vary from seconds to hundreds of years, especially for die-level failure mechanisms such as EM, TDDB, HCI, and NBTI [20]. In such conditions, even the

accelerated tests could not provide results as the acceleration factor (AF) will be so high that the failure mechanism to be tested will not remain the same. Also, testing must be performed for each failure mechanism for a part that requires different test setups. In addition, to complete part selection based on reliability for "n" number of parts for "m" number of failure mechanisms, the number of tests, testing setups, and the length of test till failure is so huge that companies will be out of the market by the time they finish performing the testing. Moreover, the part manufacturers do not provide the test methods, number of samples, sample size, failure criteria, and other critical information required to perform testing [14]. In conclusion, testing the samples is not a solution to achieving part selection based on reliability.

1.2.3. Refusing to Divulge Information

Apart from the concerns mentioned above, there are additional aspects for which the information is labeled as proprietary, which cannot be shared or considered a business secret in the PPAP document. For the same part mentioned in the reported PPAP, the die channel length is regarded as confidential information as per Texas Instruments, which is not provided, as shown in Figure 5. Understanding the die channel length is one of the preliminary steps in performing a part reliability assessment which will be discussed in Chapter 4.

Wafer / Die Technology Description:	
a. Wafer / Die process technology:	3310LBC5X.03
b. Die channel length:	TI Confidential - NDA Restrictions
c. Die gate length:	0.4um

Figure 5: Wafer/die technology description provided in the PPAP document [14].

1.2.4. PPAP Availability

In addition, not all part manufacturers provide the PPAP document. Of the ten parts used for the study, only 1 part manufacturer provided the PPAP document. While some manufacturers do

or may provide the information upon request, it depends on the scale at which the parts are purchased from the manufacturer. There will be some instances in which the manufacturer may not respond or does not want to provide the information. This was evaluated by analyzing all of the MOSFETs provided on the Diodes Inc. website [21].

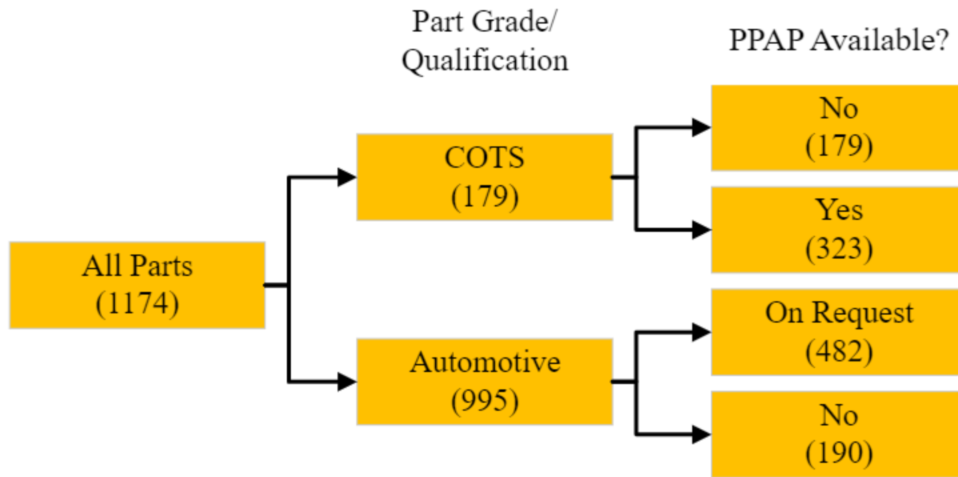


Figure 6: Availability of PPAP documentation for Diodes Inc. MOSFETs [22].

Diodes Inc. has 1174 MOSFETs, 179 of which are rated as commercial (COTS), and the remaining 995 are automotive parts. Figure 6 shows the results of the analysis. Of the automotive parts, 19% do not provide a PPAP document, 48% provide a PPAP document with an additional request, and the rest have a direct link to the PPAP document [22]. To summarize, the PPAP could be a good resource of information related to a part that in itself is limited to providing the bare minimum data, and one may not find it for a few other parts at all.

1.3. Potential Recommendations Based on Observations

In summary, the issue of part manufacturers avoiding conveying useful information is a challenge requiring proactive measures. Highlighting the importance of effective communication and transparency throughout the supply chain is vital. Manufacturers should recognize that

providing useful information enhances trust, strengthens relationships, and ultimately benefits their long-term reputation and customer satisfaction. Clear guidelines and contractual agreements must be established to ensure manufacturers fulfill their obligations to convey comprehensive and relevant information to customers.

Furthermore, customers should actively engage with their suppliers and express their expectations regarding information exchange. Customers can encourage manufacturers to be more forthcoming with valuable information by clearly articulating their needs and requirements. Collaboration and open dialogue between manufacturers and customers can help build mutual understanding and enable the development of effective solutions that address concerns while respecting proprietary rights and competitive considerations. Regulatory bodies and industry associations also play a vital role in addressing this issue. Organizations such as JEDEC, International Electrotechnical Commission (IEC), and AEC can establish guidelines, standards, and best practices that promote transparent information exchange between manufacturers and customers. Regular audits and inspections can be conducted to ensure compliance and discourage the practice of avoiding conveying useful information. By fostering a culture of transparency, standardized procedures, and open communication, manufacturers can fulfill their responsibility to provide comprehensive information while protecting their legitimate interests. Performing these will ultimately contribute to better decision-making, enhanced product quality, and stronger relationships between manufacturers and customers.

2. Unmasking the Limitations of Industry-Published Documents on Die-Level Failure Mechanism Models Concerning Time-to-Failure Estimation

The focus of this project was not on developing a new model for die-level failure mechanisms. Instead, my exploration began by delving into industry-published documents specifically addressing failure models at the die level. I aimed to thoroughly examine the available information sources and determine how the models can be utilized in modeling part selection. By carefully analyzing these documents, I hoped to gain valuable insights into the various models of failure mechanisms, such as Time-Dependent Dielectric Breakdown (TDDB), Electromigration (EM), Hot Carrier Injection (HCI), and Negative Bias Temperature Instability (NBTI). I recognized that the existing industry literature JEDEC JEP122H: Failure Mechanisms and Models for Semiconductor Devices [23], might provide valuable knowledge and insights regarding these failure mechanisms. However, my primary objective was to understand the extent to which industry-published documents discuss these mechanisms and the applicability of failure models. Specifically, I aimed to investigate whether these documents shed light on time-to-failure analysis, which is crucial in evaluating the reliability and durability of semiconductor devices at the die level.

This chapter details the four die-level failure mechanisms (EM, TDDB, HCI, and NBTI) and respective failure models. By scrutinizing the available source of information, I aimed to uncover any potential gaps or limitations in the JEP122H standard of these failure mechanisms and assess the feasibility of utilizing existing models for my research and modeling part selection.

2.1. Literature Review of Failure Mechanisms and Models

Advanced integrated circuits (ICs) are characterized by complex designs and usage of a wide variety of materials, including semiconductors, insulators, metals, and plastic molding compounds, among others [24]. The success of semiconductors has been significantly attributed to the critical role played by the scaling of device geometries, which has led to improved performance and cost reductions per device [25]. The process of scaling, which involves reducing device geometries by 0.7x for each new technology node following Moore's Law, has resulted in an increase in electric fields within materials [26]. This has brought the materials closer to their breakdown strength and has led to concerns regarding electromigration (EM) due to the rise in current densities in metallization. The acceleration of reliability issues, such as time-dependent dielectric breakdown (TDDB), hot-carrier injection (HCI), and negative-bias temperature instability (NBTI), can occur with higher electric fields, as elaborated in the sections that follow [27]. These failure mechanisms in complementary metal-oxide-semiconductor (CMOS) are illustrated in Figure 7.

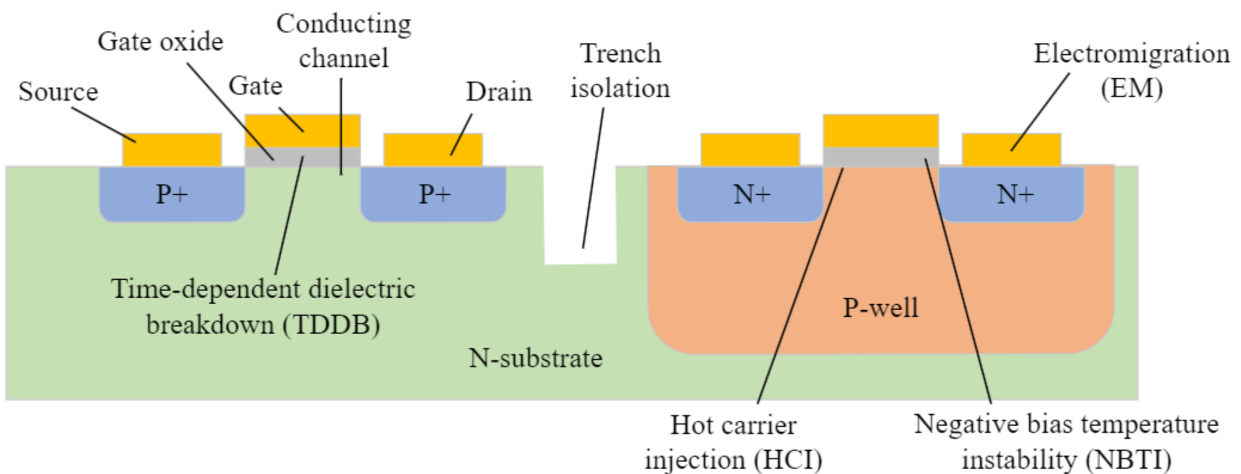


Figure 7: CMOS wearout die-level failure mechanisms [28].

2.1.1. Electromigration

Electromigration is a critical reliability concern in CMOS devices. Electromigration is when the formation of a high current density, caused by local heating, parasitic currents, and other sources, results in the flow of metallic atoms in the direction of current flow [29]. This flow of metallic atoms over time impacts electronic function over time. The flow of metallic atoms essentially causes the formation of voids in some areas of the overall lattice (potentially leading to open circuits) and the nucleation of denser metallic layers leading to the formation of hillocks (potentially leading to short circuits) [30]. Figure 8 demonstrates the electromigration process.

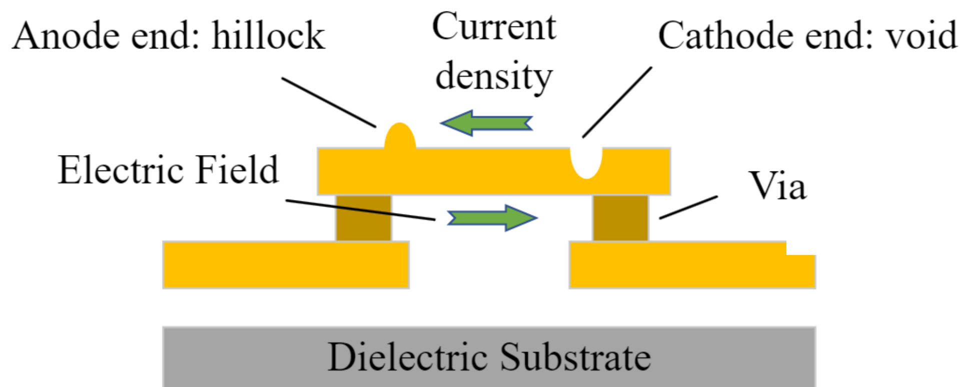


Figure 8: Illustration of void and hillock due to electromigration in interconnects [31].

The electromigration failure mechanism, as shown in Figure 9, begins due to the momentum exchange between the current-carrying electrons and the metal lattice. For high-electron current densities, the electron wind (collisions of the electrons with the metal ions in the lattice) serves to exert force on the metal ion, which is large enough to cause the metal ion to drift [32]. Generally, this metal-ion movement is along grain boundaries in aluminum (Al)-alloys and along interfaces for copper (Cu) [33].

Along with the electron wind and interconnect material, flux divergence is a critical element of the electromigration failure mechanism [34]. Flux divergence represents the net flow of material into and out of a region of interest (interconnect length). A flux divergence can result in the accumulation or depletion of metal ions in the region of interest. Microstructure differences, such as grain size differences, result in flux divergences. Electromigration-induced transport is primarily along grain boundaries in polycrystalline Al-alloy conductors. Grain boundaries in an interconnect are usually not uniform which is illustrated as two regions of uniform grain structure in Figure 9 for simplicity [35]. Electron flow from left to right can serve to produce a void in the metal due to the flux divergence at the microstructure gradient. Electron flow from right to left can produce an accumulation of metal due to the flux divergence at the microstructure gradient. The void or accumulation (hillock) primarily initiates at triple points of grain boundaries. The dominant electromigration-transport mechanism for Cu can be along the Cu barrier interfaces.

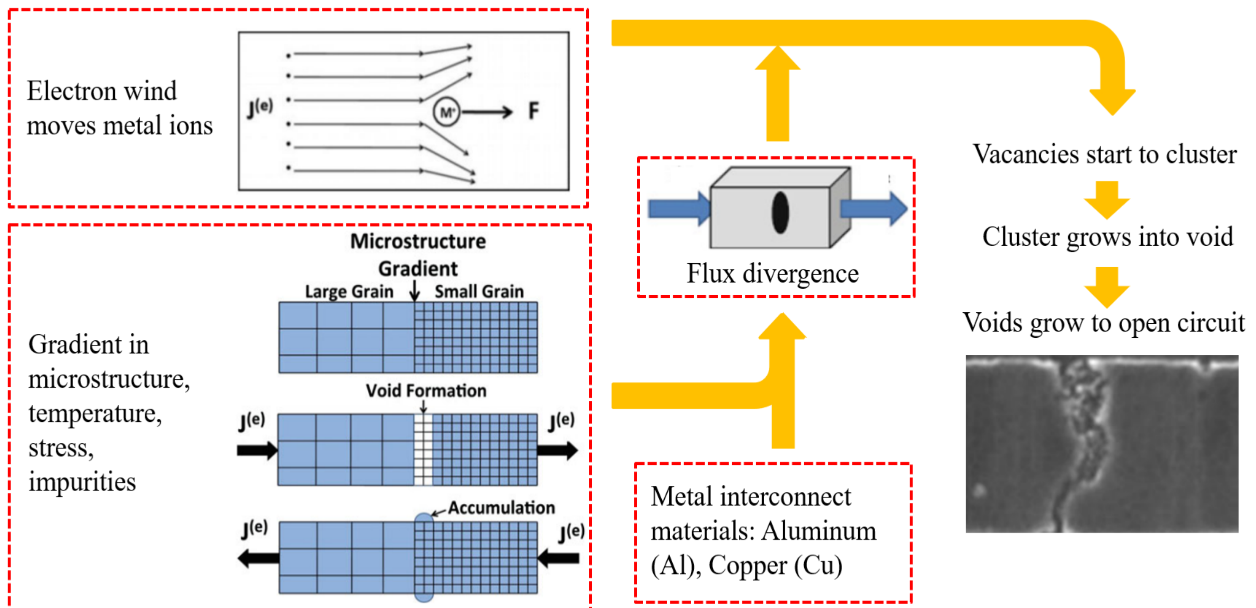


Figure 9: Failure mechanism of electromigration [35].

Failures caused by electromigration in CMOS include open circuits and shorts [36]. Open circuits occur when the metal line breaks due to voids, leading to a discontinuity in the electrical path. Shorts occur when adjacent metal lines come into contact due to metal accumulation or the formation of hillocks. The metal accumulated can break through the dielectric separating the adjacent interconnects resulting in unintended electrical connections. An increase in resistance can cause performance degradation in the IC resulting in slower signal transmission, increased power consumption, and reduced overall circuit functionality.

To detect and analyze electromigration failures, various techniques are employed [37]. One common method is electrical testing, where the resistance of metal lines is monitored over time. An increase in resistance can indicate the thinning or breakage of metal lines. Additionally, techniques such as current stress tests are used to evaluate the reliability of CMOS devices under accelerated aging conditions. Failure analysis techniques, such as scanning electron microscopy (SEM), transmission electron microscopy (TEM), and focused ion beam (FIB), are utilized to analyze the failed metal lines and identify the root cause of the failure. SEM and TEM allow for visualizing voids, metal thinning, and other structural changes [38]. FIB is used for cross-sectional analysis, enabling precise imaging, and probing of the failed region.

Design tools and techniques are employed to protect against electromigration failures in CMOS devices. Proper material selection is crucial, with copper and copper alloys being preferred over aluminum due to their better resistance to electromigration [39]. Design rules are optimized to ensure appropriate line widths and thicknesses, minimizing the current density and reducing the susceptibility to electromigration. Selecting dielectric materials with low diffusion rates, such as low-k dielectrics, and using barrier layers and passivation materials to prevent metal diffusion into the surrounding dielectric materials improves the reliability of interconnects

[40]. Stress engineering techniques, such as introducing compressive or tensile stress in the metal lines, can enhance their resistance to electromigration-induced failures.

The PPAP provided JEDEC JESD61A: Isothermal Electromigration Test Procedure as test specification for electromigration qualification [41]. This document provided an accelerated current stress test, and the failure criterion is defined based on the maximum percent resistance increment of the test line. It is provided that the test is terminated in general when the maximum percent resistance increment is about 2%.

Black's equation estimates the time to failure based on the interconnect dimensions, absolute temperature, physical material properties, electron current density, and activation energy for EM to occur and an experimentally determined exponent that varies depending on the EM failure mode [23]. This model assumes that empirical values attained during accelerated testing can be applied to normal use conditions to provide a model of TTF. The model is shown in equation (1), and all the model inputs are listed in Table 1. For aluminum, the test current densities should be on or above the order of 10 mA/μm^2 (1 x 10^6 A/cm^2), the conductor should be at least 500 μm in length and preferably 1 mm long. In contrast to Al, for Cu test structure, lengths are commonly between 200 and 400 μm for stress current densities on the order of 20 mA/μm^2. The failure criterion is a fractional or percentage resistance increase (e.g., ΔR/R x 100 = 20% is commonly used).

$$TTF = \frac{A_0}{j^n} . e^{\frac{E_{aa}}{kT}} \qquad (1)$$

Table 1: Input Parameters for Black's Equation [23].

Variable	Function or Purpose	Unit	Method of Determination

A_0	Scaling Factor	(time*A)/cm^2	Experimentally determined from life testing for technology by product developers
j	Current density	A/cm^2	Calculated from applied interconnect current and cross-sectional area
n	Exponent	Constant	Experimentally determined, dependent on interconnect material, experimental conditions, and junction failure mode. Range lies between $1.1 < n < 2$, in common, Aluminum: $n = 2$ Copper: $n = 1.1$
E_{aa}	Apparent activation energy	eV	Experimentally determined, dependent on conductor diffusion pathways. Al + %Si: $0.5 < E_{aa} < 0.6$ Al + %Cu: $0.7 < E_{aa} < 0.8$ Cu: $0.85 < E_{aa} < 0.95$
k	Boltzmann's constant	eV/K	8.6173303×10^{-5} eV/K
T	Temperature	K	Application specific

2.1.2. Time-Dependent Dielectric Breakdown

Due to the very high operating electric fields in the gate dielectric of CMOS devices, time-dependent dielectric breakdown (TDDB) can be an important IC failure mechanism. Time-dependent dielectric breakdown is the failure mechanism that occurs when a constant electronic field application less than the breakdown strength of the dielectric material eventually wears down the gate oxide of a CMOS [42]. The gate oxide, typically silicon dioxide (SiO_2), serves as an insulating layer between the gate electrode and the channel region in a CMOS. TDDB refers to the degradation and eventual breakdown of the gate oxide over time under electrical stress which is caused by creating conductive paths [43].

The failure mechanism of gate oxide TDDB involves four steps, as illustrated in Figure 10 [44]. Step 1 is about the formation and growth of defects within the oxide layer due to the application of high electric fields. There are two types of defects extrinsic and intrinsic. Extrinsic defects occur due to material defects and manufacturing process-induced defects. Intrinsic defects are created while operating as the defects flow around in the gate oxide, the electrons at the gate/gate oxide interface can leak through the interface using the extended defects or traps, leaving a hole inside the gate oxide. These defects, known as traps, can capture and release charge carriers leading to an increase in the number of traps inside the gate oxide. Over time, the cumulative effect creates a conduction path for the charge carriers to flow through the gate oxide, as in Step 2. This leakage current or charge carriers flowing through the conduction path further increases the number of defects due to thermal damage, which creates more paths leading to thermal runaway, as shown in Step 3, also known as a soft breakdown. With an increase in temperature due to thermal runaway, the gate oxide (SiO_2) melts, leaving a conduction channel through breakdown as shown in Step 4, also identified as hard breakdown.

The steps that occur during the failure mechanism of TDDB are explained through the gate current vs. stress time plot, as shown in Figure 11 [45]. Due to the presence of extrinsic defects, there is a leakage current right from the beginning, as shown in Step 1, but the leakage current increases slightly over time due to extra traps that are created over time. Step 2 shows a sudden spike in leakage current as the conduction path is created during this phase. Step 3 shows an increase in leakage current due to thermal runaway, also called soft breakdown. There are two soft breakdowns in the plot suggesting that two conduction channels are simultaneously created during the stage at different locations of the gate oxide. Step 4 has the spike in leakage current

representing the gate oxide hard breakdown or channel creation through the oxide, as shown in the neighboring microscopy images.

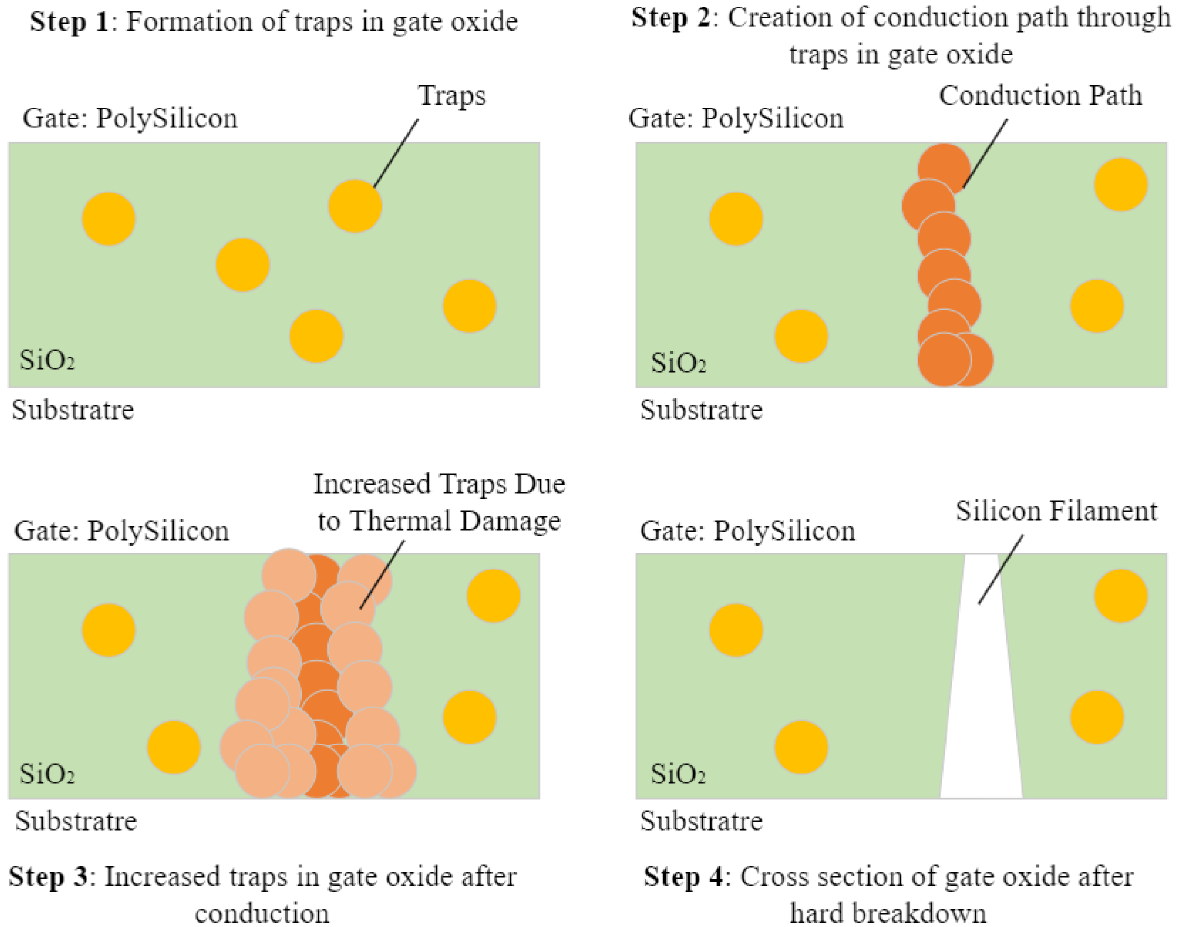


Figure 10: TDDB failure mechanism process steps [44].

Failures caused by gate oxide TDDB include oxide breakdown and gate leakage. Oxide breakdown occurs when the gate oxide layer cannot withstand the applied voltage, forming a conductive path through the oxide [46]. This leads to an unintended electrical connection and can cause device malfunctions or failures. Gate leakage refers to the undesirable current flow through the gate oxide, which can adversely affect device performance and increase power consumption.

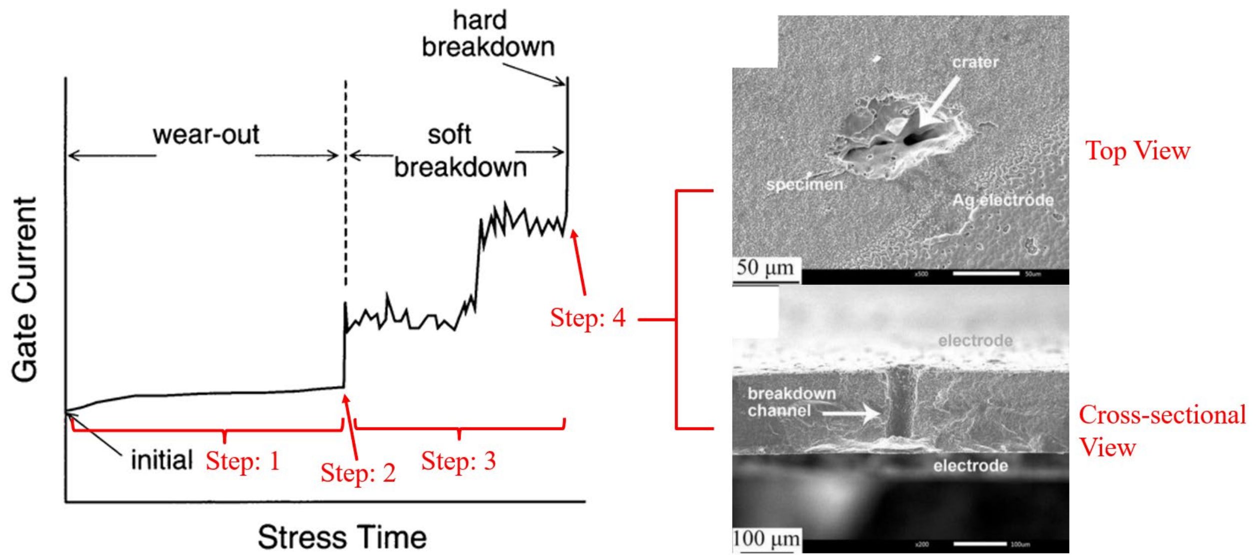


Figure 11: TDDB failure mechanism explained through gate current vs stress time plot [45].

Accelerated stress tests are performed on samples to detect and analyze gate oxide TDDB failures. These tests involve subjecting the devices to high electric fields and monitoring their degradation over time. The devices are typically stressed under high voltage, which accelerates the TDDB process. Electrical measurements, such as time-dependent leakage current measurements and breakdown voltage measurements, are used to assess the reliability and lifetime of the gate oxide [47].

Failure analysis techniques, including electrical characterization, microscopy, and spectroscopy, are employed to analyze the failed gate oxide [48]. Techniques such as scanning electron microscopy (SEM) and transmission electron microscopy (TEM) are used to visualize the defects and structural changes within the oxide layer. Additionally, techniques like Fourier-transform infrared (FTIR) spectroscopy and secondary ion mass spectrometry (SIMS) can provide valuable information about the chemical composition and elemental distribution within the gate oxide.

Design tools and techniques are employed to protect against gate oxide TDDB failures. Proper material selection is crucial, with the choice of high-quality silicon dioxide (SiO_2) or advanced gate dielectric materials like high-k materials with superior TDDB characteristics [49]. Optimized design rules are implemented to ensure appropriate oxide thickness and gate geometry, reducing the electric field and stress within the oxide. Stress engineering techniques, such as introducing strain in the channel region, can also improve the reliability of the gate oxide [50]. Cooling techniques and thermal dissipation within the ICs are implemented to maintain lower operating temperatures and improve reliability as temperature rise accelerates TDDB failures. Control of deposition, annealing conditions, and reduction of impurities or defects in the dielectric layer are important process considerations.

The PPAP provided JEDEC JESD35A: Procedure for the Wafer-Level Testing of Thin Dielectrics as test specifications for TDDB qualification [51]. This document provided ramped voltage, constant voltage, and ramped current stress tests. No failure criterion is defined in the standard, and it is explicitly mentioned that ″the purpose of this document is to describe oxide test techniques for quick evaluation and control of oxide fabrication techniques. It does not specify acceptance or rejection criteria for any of the described procedures and, therefore not intended to be used to predict MOS Integrated Circuit failure rates."

TDDB models are mathematical representations that estimate the time to failure of the gate oxide due to dielectric breakdown. These models are intended for silicon dioxide gate dielectric application over a range of oxide thicknesses. The physical models used to explain the four empirical models are the thermo-chemical model (E model or constant field/voltage acceleration exponential model), anode hole injection (1/E model or, equivalently, anode hole injection model), bulk trap generation (V model, where the failure rate is exponential with voltage), and

anode hydrogen release model (Anode hydrogen release for the power-law model) [23]. While the thermo-chemical and V models adopt a field-driven mechanism, both anode hole injection and anode hydrogen release models assume a current-driven mechanism in addition to the role of the applied voltage or oxide fields, depending on the specific conditions. Based on the existing literature and the standards, E and 1/E models best correlate for estimating the TDDB failures which are discussed in this section.

In the E model, as shown in equation (2), for gate oxide thickness greater than 4 nm, TDDB is due to field-enhanced thermal bond breakage at the silicon-silica interface. The E-field reduces the activation energy required for thermal bond breakage and exponentially increases the failure reaction rate. The time-to-failure (TTF), inverse to reaction rate, decreases exponentially with temperature. The inputs required for the E model are provided in Table 2.

$$TTF = B_0 \exp\left(-\gamma \frac{V_g}{t_{ox}}\right) \exp\left(\frac{E_a}{kT_j}\right) \tag{2}$$

Table 2: Input Parameters for the E model [23].

Variable	Function or Purpose	Unit	Method of Determination
B_0	Scaling factor	times	Experimental results
γ	Field acceleration constant	cm/MV	Industry standards or literature. Range in $2.5 < \gamma < 3.5$
V_g	Gate voltage	V	Application specific
t_{ox}	Gate oxide thickness	nm	Part Specific

Variable	Function or Purpose	Unit	Method of Determination
E_a	Apparent activation energy for TDDB	eV	Industry standards or literature. Range in $0.6 < E_{aa} < 0.9$
T_j	Junction temperature	K	Application specific
k	Boltzmann's constant	eV/K	8.6173303 × 10^{-5} eV/K

The 1/E model, as shown in equation (3), for gate oxide thickness less than 4 nm, assumes the cause of TDDB (even at low fields) is postulated to be due to current through the dielectric by Fowler-Nordheim (F-N) conduction. F-N injected electrons (from the cathode) cause impact ionization damage of the dielectric due to accelerating through the dielectric. When these accelerated electrons reach the anode, hot holes may be produced that can tunnel back into the dielectric, causing damage (hot-hole anode injection mechanism). The time-to-failure is expected to show an exponential dependence on the inverse of the electric field. The inputs required for the 1/E model are provided in Table 3.

$$TTF = \tau_0(T) \exp\left(\frac{G(T) t_{ox}}{V_g}\right) \quad (3)$$

Table 3: Input Parameters for 1/E model [23].

Variable	Function or Purpose	Unit	Method of Determination
$\tau_0(T)$	Scaling factor	seconds	Industry standards or literature. Approximately 1 x 10^{-11} s

Variable	Function or Purpose	Unit	Method of Determination
$G(T)$	Field acceleration constant	MV/cm	Industry standards or literature. Approximately 350 MV/cm
V_g	Gate voltage	V	Application specific
t_{ox}	Gate oxide thickness	nm	Part Specific

2.1.3. Hot Carrier Injection

Hot carrier injection is a reliability concern in CMOS technology that can lead to device degradation and failure. It occurs when high-energy carriers, typically electrons or holes, gain sufficient kinetic energy and impact the gate oxide, causing damage to its structure and properties. The primary cause of hot carrier injection is the presence of high electric fields in the transistor channel region [52]. This occurs as carriers move along the channel in CMOS and experience impact ionization near the drain end of the device, as shown in Figure 12 [53]. The damage can occur at the interface, within the oxide and/or within the sidewall spacer.

The silicon–silicon dioxide interface shown in Figure 13 is critical to undergoing failure mechanism [35]. Silicon atoms in the substrate are four-fold bonded in a crystalline lattice. The SiO_2 layer is amorphous, with the silicon four-fold bonded to neighboring oxygen (in a tetrahedral arrangement). Due to lattice mismatch at the interface, not all silicon bonds will be satisfied, creating dangling silicon bonds. Hydrogen is usually introduced during CMOS fabrication to chemically tie up/terminate these dangling bonds and prevent them from being electrically active.

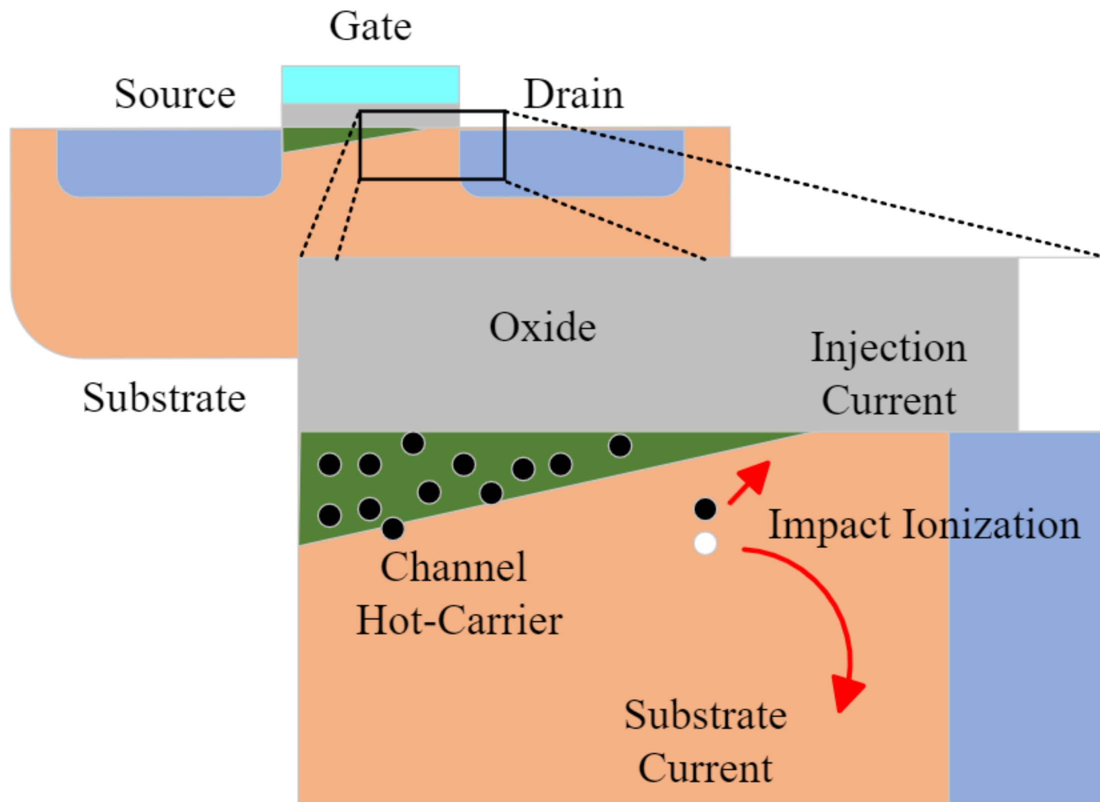


Figure 12: Cross-section of an n-channel MOSFET illustrating the generation and injection of hot carriers into the gate-oxide (SiO_2) [53].

As electrons are accelerated from the source to the drain in the electric field, impact ionization at the drain end of the CMOS can produce electron–hole pairs. The electrons are redirected towards the gate oxide under the influence of the strong electric field near the drain end of the channel. The channel is not a perfect rectangular path but a tapered path, as shown in Figure 14 [54]. The energetic electrons, redirected toward the Si/SiO_2 interface, produce interface damage in a localized region near the drain end (Si-H bond breakage), reducing its electrical performance and overall reliability. Over time, this damage accumulates and results in threshold voltage shift, increased leakage current, or even gate oxide breakdown.

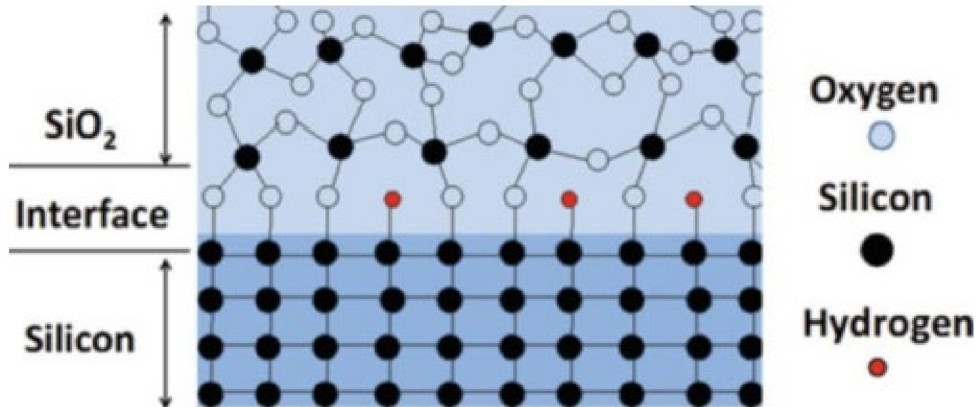


Figure 13: Si – SiO_2 interface [35].

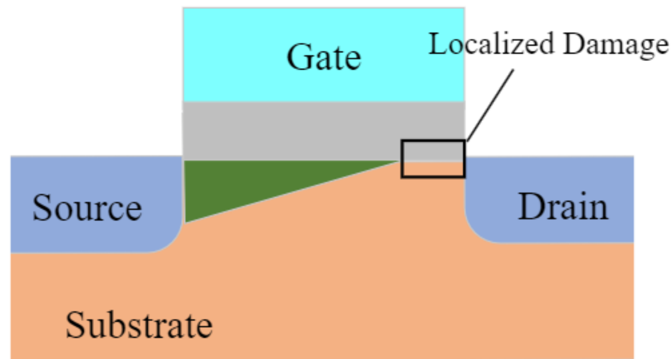


Figure 14: Drain end of the channel producing electron-hole pairs [54].

Failures caused by gate oxide hot carrier injection include degradation of transistor parameters, such as threshold voltage shift and subthreshold slope degradation. Threshold voltage shift refers to the change in the voltage required to turn on or off the transistor, affecting the device's operational characteristics [55]. Subthreshold slope degradation relates to the increase in the off-state leakage current, which reduces the overall efficiency and increases power consumption.

Unlike other failure mechanisms, HCI-induced damage does not typically result in visible physical changes or visible signs of failure on the device surface. Instead, electrical

measurements and characterization primarily detect and analyze HCI failures [56]. This involves evaluating the electrical performance of the affected transistors or circuits, such as threshold voltage shifts, subthreshold slope degradation, or increased leakage currents. These electrical changes are indicators of the impact of HCI on the device's functionality and reliability. Techniques like transient current measurement, time-dependent degradation measurement, and stress tests can be performed to investigate HCI-induced failures further. These techniques involve subjecting the device to specific electrical conditions and monitoring its response over time. By observing the device's electrical behavior under different stress conditions, analysts can gain insights into the extent of HCI-induced degradation and the device's reliability [57].

Design tools and techniques are implemented to protect against gate oxide hot carrier injection. One approach is optimizing transistor dimensions and channel doping profiles to reduce the electric fields in the channel region. Using lightly doped drain (LDD) or double doped drain (DDD) structures or extension implants such as side walls can help distribute the electric field more uniformly and mitigate the impact of hot carriers on the gate oxide [58]. Additionally, advanced device structures, such as strained silicon or high-k dielectrics, can improve the resistance to hot carrier injection.

HCI evaluations are almost always performed on test structures rather than products and done under direct current (DC) conditions, thus, the calculated lifetime should be considered a figure of merit for process comparison [59]. A short lifetime observed with DC test structures does not imply unacceptable product performance under alternating current (AC) conditions. For a digital circuit, like an inverter, HCI stress only occurs during the device's turn-on and turn-off periods. These turn-on and turn-off periods are typically 1-2% of the overall cycle time. Thus, the time to failure (TTF) due to HCI under usage stress conditions is significantly lower than the

predicted TTF under DC conditions. HCI is considered a critical failure mechanism or tends to increase the time to failure for advanced process technologies, such as below 130 nm. As technology nodes shrink and operating voltages increase, the electric fields in the channel region intensify, making the gate oxide more susceptible to hot carrier injection.

The PPAP provided JEDEC JESD28A and 60A: A Procedure for Measuring N and P-Channel MOSFET Hot-Carrier-Induced Degradation Under DC Stress as test specifications for HCI qualification [60], [61]. No failure criterion is defined in these standards, and it is explicitly mentioned that ″These are to be used for comparison purposes only and should not be used as acceptance or rejection criteria. It is also important to realize that this procedure should not be interpreted to predict MOS IC failure rates."

HCI-induced transistor degradation is well modeled by peak substrate current for the n-channels and peak gate current for the p-channels, at least for transistors at >0.25 µm gate length (L). For <0.25 µm p-channel, the worst-case lifetime occurs at maximum substrate current stress, and the time-to-failure (TTF) model is the same as the n-channel. The time to failure for HCI can be obtained from equation (4), and the input parameters are listed in Table 4.

$$TTF = C_0 (I)^{-n} e^{\frac{E_{aa}}{kT}} \quad (4)$$

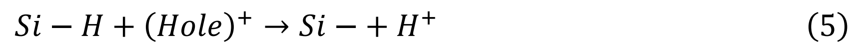
Table 4: Input Parameters for HCI time to failure model [23].

Variable	**Function or Purpose**	**Unit**	**Method of Determination**
C_0	Scaling factor	times	Experimental results
$I = I_{sub}$	Substrate current	µA	For N-channel, Measure peak substrate current during stressing or estimate based on information from datasheet

Variable	Function or Purpose	Unit	Method of Determination
$I = I_G$	Gate current	μA	For P-channel, Measure peak gate current during stressing or estimate based on information from datasheet
n	Empirically exponent	Constant	Function of stress voltage, temperature, and effective transistor channel length Common range is between 2 to 4
E_{aa}	Apparent Activation Energy for HCI	eV	Industry standards or literature. For N − channel: $-0.2 < E_{aa} < 0.4$ For P − channel: $(L > 0.25\mu m): -0.1 < E_{aa} < -0.2$ $(L < 0.25\mu m): 0.1 < E_{aa} < 0.4$
T	Operating temperature	K	Application specific
k	Boltzmann's constant	eV/K	8.6173303×10^{-5} eV/K

2.1.4. Negative Bias Temperature Instability

Negative Bias Temperature Instability (NBTI) is a phenomenon that affects the reliability and performance of p-channel transistors in CMOS technology. As mentioned in HCI, the dangling bonds are bonded with hydrogen during the manufacturing or fabrication process. Since the P-type MOS operates with a negative gate voltage, the electric field in the SiO_2 layer is directed away from the Si and SiO_2 interface, as shown in Figure 15 [35]. If a Si–H bond is broken during device operation by capturing a hole from the channel, it leads to freeing an H+ ion, as shown in equation (5).



$$Si - H + (Hole)^{+} \rightarrow Si - + H^{+} \quad (5)$$

Once H+ ions are generated, they drift away from the interface under the influence of an electric field governed by the transport equation as shown in equation (6), where $J(x,t)$ is the total flux, μ is the mobility, ρ is the density of H^+ ions, qE is the force acting on H^+ ions, and D is the diffusivity.

$$J(x,t) = \mu\,\rho(x,t)\,(qE) - D\frac{\partial\rho(x,t)}{\partial x} \tag{6}$$

The total flux equation can also be expressed as a drift and diffusion flux change, as shown in Figure 16. Drift flux occurs as the free H^+ ions move under the influence of the electric field into the gate oxide from the interface. This increases the concentration of the H^+ ions in the gate oxide. When the electric field is not applied, due to the higher concentration, the H^+ ions diffuse to the lower concentration areas (gate oxide interface), and re-bond with the silicon atoms which is represented by the diffusion flux. This leads to the recovery of the gate oxide properties by reducing the number of traps that are created during the application of the electric field. But the recovery is partial because of the H^+ ions reacting with the already present traps, as shown in equations (7), (8), and (9).

In summary, there are two modes in the NBTI failure mechanism: the stress condition mode and the recovery mode, as shown in Figure 17 [62]. The stress condition is when the electric field is applied, leading to hole trapping and bond breakage. The recovery mode is when no electric field is applied, due to which the bonds are partially rejoined.

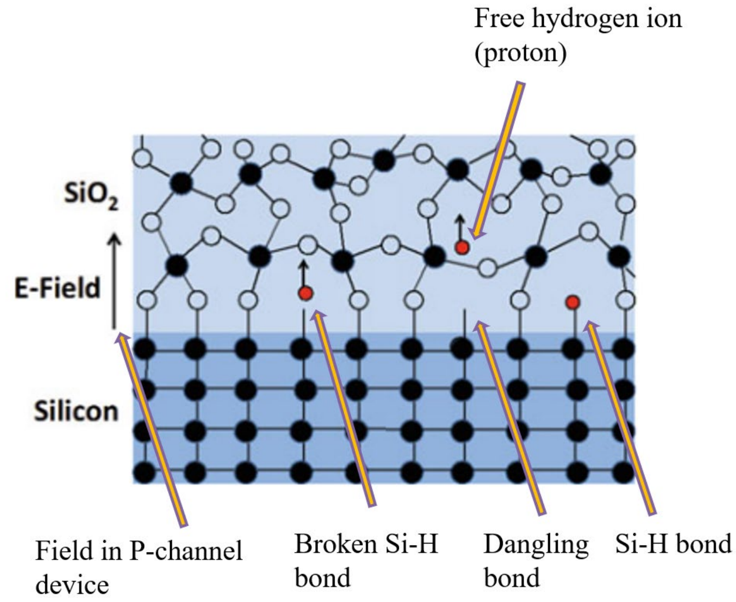


Figure 15: NBTI failure mechanism through Si/SiO_2 interface [35].

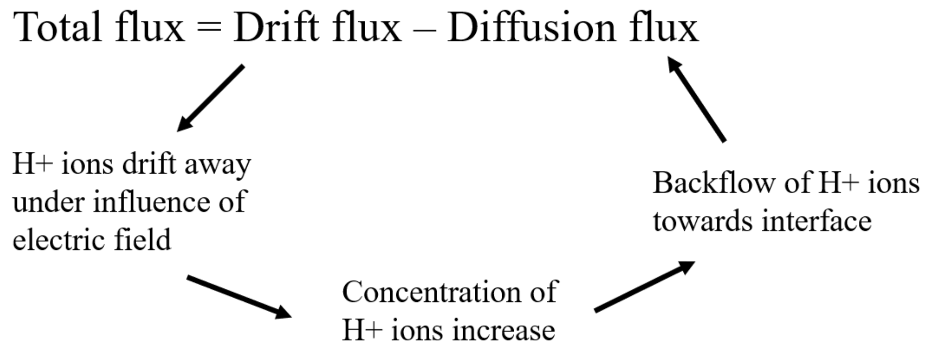
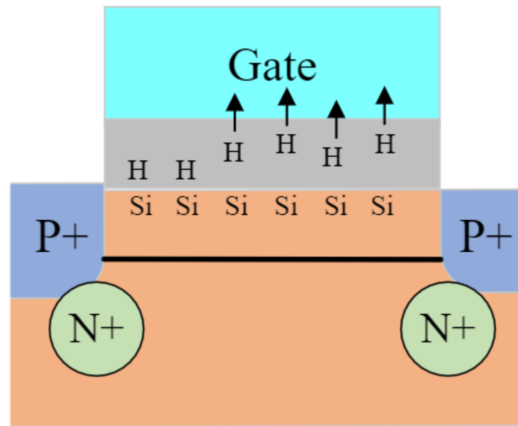


Figure 16: Partial recovery of the gate oxide in NBTI failure mechanism [35].

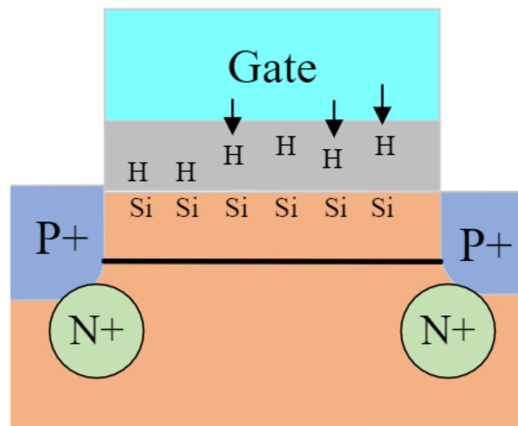
$$H^{+} + e \rightarrow H \tag{7}$$

$$H^{+} + H + e \rightarrow H_2 \tag{8}$$

$$H^{+} + H^{+} + 2e \rightarrow H_2 \tag{9}$$



(a) Stress Condition



(b) Recovery

Figure 17: Cross-section of pMOS device under (a) NBTI stress conditions (b) in recovery [62].

NBTI involves the trapping and de-trapping positive charges in the gate oxide of p-channel transistors under negative bias and elevated temperature conditions [63]. The trapped charges cause a degradation in the transistor's characteristics, leading to increased threshold voltage and reduced channel mobility. This results in decreased device speed, increased power consumption, and timing violations in CMOS circuits. Examples of NBTI failures can be observed in various scenarios. In a digital circuit, the increased threshold voltage can cause a delay in signal propagation, impacting overall circuit performance. In analog circuits, NBTI-induced threshold

voltage shifts can result in offset voltage variations and reduced gain, compromising the accuracy and linearity of the circuit [64]. These failures manifest as performance degradation, reduced reliability, and potential functional failures in CMOS devices.

The detection and analysis of NBTI failures involve several techniques. Stress testing methodologies, such as applying negative bias and elevated temperature for extended periods, accelerate the degradation process. Electrical measurements, such as monitoring threshold voltage shifts over time, provide valuable insights into the extent of NBTI-induced degradation. Statistical analysis and modeling approaches are employed to predict the reliability and lifetime of devices under NBTI stress conditions.

To protect against NBTI failures, design tools and techniques are employed during the fabrication and design stages. Stress engineering involves optimizing the transistor's gate stack and process parameters to mitigate NBTI effects. Channel engineering techniques, such as using stress liners and embedded silicon-germanium (SiGe), help enhance the channel's resistance to NBTI-induced degradation. Material selection, such as high-k dielectrics for gate oxides, can reduce NBTI susceptibility. Design rules are optimized to minimize the impact of NBTI during layout and ensure robustness against NBTI-induced failures.

Unlike the other failure mechanisms (EM, TDDB, and HCI), the PPAP document does not provide any specification for NBTI, which leads to no conclusions about how the part has been tested and qualified for NBTI as there is no information about the testing methods, failure criteria, number of samples tested, failure times, testing data, and many more.

Although there are disagreements about the physical mechanism behind the degradation and the exact cause of bias temperature instability, two effects are believed to be at play: trapping positively charged holes and generating interface states [23]. It has been found that a broad

consensus is that when a MOS is stressed with a constant gate voltage at an elevated temperature, positive charges accumulate in the SiO_2/Si interface or gate oxide layer. This charge leads to the deterioration of transistor parameters. The knowledge of physics limits the current state of the NBTI models for this mechanism. For a given gate oxide thickness (t_{ox}), either one of the equation (10) or (11) phenomenological models is generally used to describe the NBTI degradation.

$$\Delta p = D_o \exp\left(\frac{E_{aa}}{kT}\right) \exp\left(\beta V_g\right) t^n \tag{10}$$

Thus, time-to-failure (TTF) for a given accepted Δp failure criterion (Δp_t), is

$$TTF = \left[\frac{\Delta p_t}{D_0 \exp\left(\frac{E_{aa}}{kT}\right) \exp\left(\alpha V_g\right)}\right]^{\frac{1}{n}} \tag{11}$$

The failure criterion Δp_t is defined in terms of an allowed pMOS parameter shift. Typically, selecting a given failure criterion should depend on the circuit sensitivities and requirements of the pMOS device under investigation.

Table 5: Model parameters for NBTI failure mechanism [23].

Variable	Function or Purpose	Unit	Method of Determination
D_0	Scaling factor	times	Pre-factor is dependent on the gate oxide process and CMOS technology. Obtained from experimental results.
Δp_t	The shift in device parameter of interest (threshold voltage (V_T), drain current (I_{Dsat}))	Based on the parameter of interest.	-

Variable	Function or Purpose	Unit	Method of Determination
V_g	Gate voltage	V	The absolute value of the gate voltage applied to the pMOS device in inversion. Obtained from datasheet or experimental results.
α	Measured gate voltage exponent	Constant	Measured values range between 3 to 4
n	Measured time exponent	Constant	Measured values range between 0.15 to 0.25
E_{aa}	Apparent activation energy for NBTI	eV	Industry standards or literature: The typical range is 0.15 to 0.25 eV
T	Operating temperature	K	Application specific
k	Boltzmann's constant	eV/K	8.6173303×10^{-5} eV/K

2.2. Observations and Limitations

The JEP122 standard provided comprehensive information on die-level failure mechanisms (EM, TDDB, HCI, and NBTI) and their corresponding failure models. Although the models are defined with relevant information, many parameters are provided as a range of values that vary depending on the parts, technology level, application conditions, and materials. Providing a broad range of values as inputs does not give proper time-to-failure distribution estimates. The remaining parameters related to part geometry or architecture and application conditions are to be collected for each part to model TTF estimates. Apart from these, the scaling factor in every failure model is not provided because it changes for each failure mechanism and for each process technology. The units of the TTF estimates also depend on the scaling factor value which is not provided in the document.

3. Process Technology Via Part Manufacturer Documents

The process technology keeps reducing by following Moore's law, and the technologies implemented are moving towards their limitations of materials and processes [65]. This has brought about innovative design rules by companies that vary from each other. As a result, a uniform approach is not being followed as in previous generations. In the past, design rules and specifications were easier to locate. It has become increasingly difficult to keep track of the complex and varying design rules developed for various applications by different companies. This is due to the decreasing portability, universal testability, and regular public disclosure of information that the industry has lost.

The design rules help estimate the reliability of the product [66]. There are failure models through which reliability simulations may be run or calculated. However, to use them, design rules need to be inputted to provide the models with the information they need. This requirement of design rules, combined with the fact that they are now less readily available, makes it more difficult for individuals and companies to estimate the reliability of their components.

Failure models depend on parameters such as part geometry, model constants, and application conditions to estimate the part's time to failure. Identifying these parameters is critical in obtaining accurate estimates of time to failure, which provides valuable insights to perform the part selection. In addition, critical decisions can be made based on a part's geometric information, which is discussed in this chapter. This chapter provides information on process technology, its benefits, and where to obtain it. Further, to better explain the process of obtaining this information, three different procedures are provided along with a summary of various documents to identify the information.

3.1. What is Process Technology?

When speaking about semiconductors, they are often referred to by their node size by the part manufacturers. A semiconductor's node size is a measure of a technology's feature size and is also commonly referred to as process technology [67]. For example, a 32 nm node, a 32 nm process technology, and a 32 nm feature size all refer to the same semiconductor process technology. The question remains, what metric does a semiconductor's feature size refer to? The feature size is defined as the minimum length of the channel, as shown in Figure 18 [68]. Feature size is sometimes synonymous with process node, a value of lambda (in general, the length of the channel). In addition to the feature size, many other geometries and properties of a semiconductor must be considered when assessing reliability. These specifications ensure that the design will be within the restraints of the manufacturing process as well as within the boundaries of physics needed for proper device functionality. All the geometries that restrict the design are collectively called design rules [69]. Examples of common geometric design rules include but are not limited to different parts' width, spacing, and pitch.

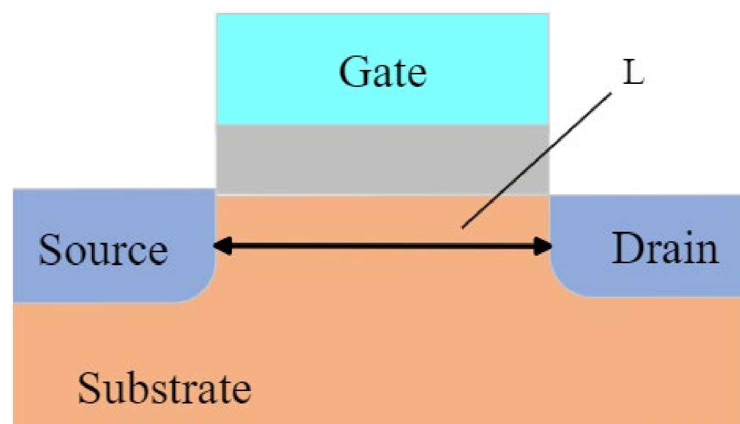


Figure 18: Physical representation of node size or process technology (L) [68].

3.2. Benefits of Obtaining Process Technology

Identifying the part process technology primarily supports decision-making on whether to consider a particular failure mechanism as critical or not. Each part consists of process technology based on which the part is manufactured [70]. As mentioned in section 2.2, failure mechanisms can be ranked, and the critical mechanisms that affect the part reliability based on process technology can be identified. Therefore, critical failure mechanisms can be identified for a given part based on the part process technology.

In addition, for a given failure mechanism, an appropriate failure model can be selected for time-to-failure estimation from various models based on process technology [71]. For example, the time-dependent dielectric breakdown mechanism has the E and 1/E failure models, as shown in section 2.1.2. Selection of the failure model for a part is performed based on the gate oxide thickness of the dielectric present between the gate and silicon substrate. If the gate oxide thickness is greater than 4 nm, the E model correlates better, and the 1/E model if less than 4 nm. In general, part manufacturers should provide gate oxide thickness. However, as discussed in Chapter 1, part manufacturers avoid providing critical information. This makes obtaining the gate oxide thickness parameter challenging. Nevertheless, knowing the process technology of part can provide insights into various geometric properties from literature sources through which a plot summary can be made to estimate the oxide thickness based on process technology.

If no part-specific information can be found for a given part, the next step is to work backward from the year of part introduction to the industry. Following Moore's Law node size scaling, which states that a transistor node size halves every two years, using the year of introduction (adjusted by two years for design and development time), one can estimate the transistor node size [72]. By surveying similar products from the same year of introduction, one

can estimate the product characteristics and use them in further failure analysis. Figure 19 shows an example of this method. Additionally, by looking at research papers from the year of introduction, one can extract information on the state of the art of product modeling at that time.

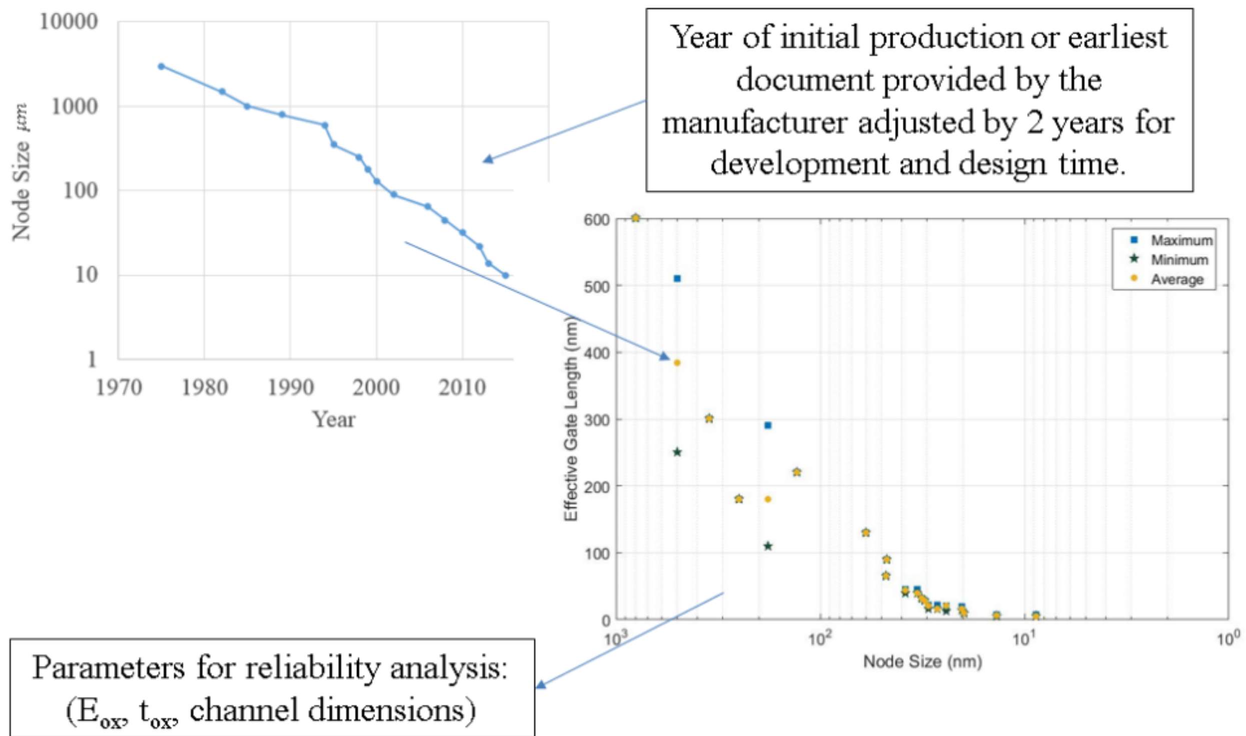


Figure 19: Using Moore's Law scaling to estimate node size and, in due course, estimate the effective gate length for the transistor.

Furthermore, industry white papers on semiconductors for process technology, as shown in Figure 20, can provide insights into geometric parameters [73]. For example, the selection of failure models for hot carrier injection mechanism is based on channel gate length. Additionally, the time-dependent dielectric breakdown E model requires a gate oxide thickness parameter as an input to estimate the time to failure. Identifying the metal interconnect thickness helps determine the occurrence of electromigration failure in the part.

	1.2µm 5volts	Units
Metal I or II pitch (width/space)	1.2 / 1.2	µm
Metal III pitch (width/space)	5.0 / 5.0	µm
Poly pitch (width/space)	1.2 / 1.2	µm
Contact	1.2 x 1.2	µm
Via 1 & 2	1.4 x 1.4	µm
Gate geometry	1.2	µm
N-well junction depth	4.0	µm
P-well junction depth	4.0	µm
N+ junction depth	0.20	µm
P+ junction depth	0.31	µm
Gate oxide thickness	225	Å
Inter poly oxide thickness	390	Å

Figure 20: Industry white paper providing information for the 1.2 µm CMOS process family [73].

Overall, understanding the process technology provides insights into other geometry or physical parameters that help create a list of mechanisms and requirements that optimizes the time and efforts towards performing reliability assessment. In further steps, process technology can be used to identify the critical failure mechanisms for a given process technology and selection of appropriate failure model for the failure mechanism specific to the part. Moreover, few failure models require geometric parameters as inputs to estimate the time to failure. Therefore, understanding the process technology of a given part is critical to perform reliability assessment and part selection.

3.3. Sources to Obtain Process Technology

To gather information about each part that is intended for application, the user has to investigate two main sources of information. These two sources of information are documents directly supplied by the manufacturer and the estimation of characteristics using related parts from a literature survey. Table 6 shows an example of part information sources.

Table 6: Example of part information sources.

<table>
<tr><th>Source Type</th><th>Data Source</th><th>Information Available</th></tr>
<tr><td rowspan="5">Manufacturer Data Sources</td><td>Datasheets [74]</td><td>• Part ratings (Operating conditions / Thermal information)
• Environmental ratings (Operating temperature ranges / Moisture sensitivity level)
• Characteristics curves (e.g., Junction-to-ambient thermal resistance vs. Air velocity)</td></tr>
<tr><td>Qualification Reports [75]</td><td>• Die dimensions / Design rule.
• Stress test results (e.g., High-temperature operating life)
• Ongoing reliability monitoring (FAB / Assembly process reliability data)
• Material composition</td></tr>
<tr><td>Material Declaration [76]</td><td>• Material composition by part structure
• Environmental rating (RoHS / REACH)</td></tr>
<tr><td>Product Change Notifications (PCN) [54] [77]</td><td>• Material composition
• Part structure / Packaging
• Qualification results</td></tr>
<tr><td>Production Part Approval Process (PPAP)</td><td>• Die Dimensions / Design Rule
• Material performance test (e.g., AEC-Q100 test results)</td></tr>
</table>

Source Type	Data Source	Information Available
	Reliability Reports	• Qualification summary • Material content
Other Sources	Industry Standards [23]	• Qualification testing levels, Model constants (e.g., JEP122), Literature
	Research Papers [23] [35]	• Model parameters/constants, Activation energy information, Node size, and associated part parameters

The part webpage serves as an introduction to the part and a gateway for more detailed information through downloadable documents and other linked pages. Each part manufacturer has their own style of part information page, which will vary but are usually consistent within a single manufacturer. The page traditionally features at least a link to the datasheet, some basic ratings and features, a set of documents associated with the part, and an image of the part. Unlike datasheets or other .pdf files, part information webpages are easily searchable and allow quick compilation of information. Figure 21 is an example of the Maxim part for which the process technology is identified through the reliability report obtained from the part webpage [78].

Figure 21: Process technology obtained through the *original component manufacturer (OCM) website [78].*

The classical document used for gaining part information is the part datasheet. The part datasheet outlines the performance parameters, operating conditions, physical dimensions, and other aspects depending on the type of part. Every part or family of parts will have a datasheet. Each datasheet typically includes the following sections: introduction, absolute maximum

ratings, electrical specifications, part layout, contact information, and document updates. Depending on the manufacturer, these sections will vary in name and order, but these sections at minimum, should be included in an effective datasheet. When compared to previous reports on part datasheets, datasheets now rarely include testing or quality data sections as these are in their documents. Figure 22 represents the process technology provided in datasheets of part manufacturers such as Microsemi, Actel Corporation, and Texas Instruments [79], [80], [81].

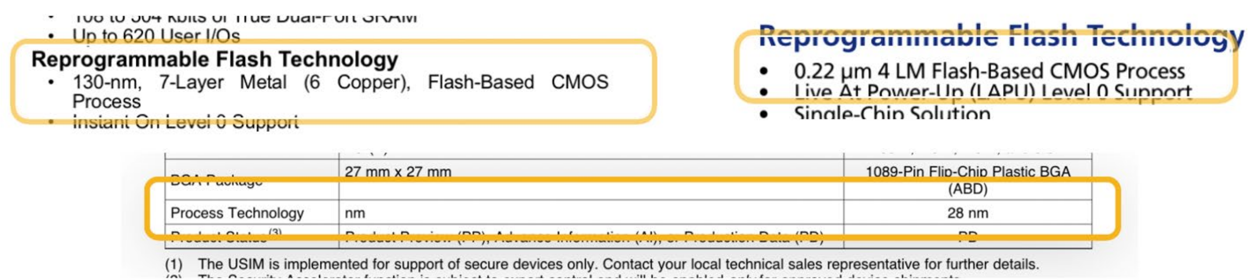


Figure 22: Datasheets of various part manufacturers as information sources for process technology [79], [80], [81].

Part manufacturers provide their customers with user guide documents, such as portfolio brochures, including critical information about the part. One such example of the part manufactured by Texas Instruments for which the process technology is obtained is shown in Figure 23 [82].

Low power consumption

The adoption of 1.2μ CMOS process technology has implemented low power consumption current characteristics. Therefore, this series is suited for portable equipment.
Static power consumption Icc (max) = 20μA

Figure 23: Process technology from user guide document [82].

Automotive parts that meet the qualification requirements of AEC (Automotive Electronic Council) must complete PPAP. This process requires documentation of a part's design, manufacture, and status to the customer. Each PPAP document contains several sections: material information, qualification testing results, and design/process failure mode effect analysis. It has

to be noted that the availability of PPAP documentation varies between parts and manufacturers. Figure 24 shows the die technology parameters provided by Texas Instruments in part PPAP document.

9. Wafer / Die Technology Description:	
a. Wafer / Die process technology:	3310LBC5X.03
b. Die channel length:	TI Confidential - NDA Restrictions
c. Die gate length:	0.4um

Figure 24: Die technology parameters provided in a PPAP document.

The qualification report for a specific part provides information about the part, including information from different tests completed on the part. This testing can include thermal, electrical, and physical testing and characterization of the part that the manufacturer completes. In addition to testing results, information about the material composition of the packaging and die structure can also be provided. Figure 25 provides the process technology/design rule for a part manufactured by TSMC, obtained through the qualification report [83].

Product Information					
Wafer Fabrication					
Factory:	CMOS:	TSMC , Taiwan	**Process:** 1P5M CMOS-8"	**Design Rule:**	0.18 um
Factory:	MEMS:	Germany	**Process** : PFD1_A	**Design Rule:**	0.25 um

Figure 25: Process technology/design rule for a part obtained through the qualification report [83].

Product Change Notifications (PCNs) are documents manufacturer issues that detail any change in the parts' construction, operation, or capabilities. PCNs can provide information regarding a change in manufacturing location, a change in material composition, or an alteration in the expected performance parameters for the part due to updated testing or other changes. Unlike datasheets or qualification reports, PCNs will typically be for a range of products provided by the manufacturer, not an individual part. At a bare minimum, a PCN must include a

unique code or number for identification, a definition or classification of the proposed part changes, the timing for the change, the deliverables to the customer, and record retention requirements. PCNs can be utilized in the part selection process for initial and long-term considerations. The initial selection process can require information only found in a PCN for the part and long-term evaluation for monitoring if the part still maintains the required performance levels for the application. For example, a PCN report on changing the process technology from 0.5 µm to 0.35 µm at a Fab location is released by TSMC [84].

Process technology for the part can be assumed from roadmaps available based on the product's year of introduction and maturity. If no part-specific information can be found for a given part, the next step is to work backward from the year of part introduction to the industry. Following Moore's Law node size scaling, which states that a transistor node size halves every two years, using the year of introduction (adjusted by two years for design and development time), one can estimate the transistor process technology. Figure 26 provides the year of introduction of process technologies [85].

Table 7 summarizes the current state of the art of selected feature sizes from 65 to 7 nm [86], [87]. The maturity of each technology is split into three categories generally:

- 'High' maturity corresponds to nodes for which semiconductor foundries are researching advanced chips for specialty applications.
- 'Moderate' maturity is associated with manufacturing facilities reporting research and development efforts towards basic process improvements or developing new lithography techniques.
- 'Low' maturity is for nodes at which full-scale manufacturing has not yet begun.

In general, foundries are working to scale these nodes to production volume within a few years. Table 7 also provides approximate market penetration figures. These estimates stem from two semiconductor foundries' annual financial reports, which provided revenue figures broken down by the wafer process node. Annual revenue totals then provided a means to estimate approximate market share relative to total FY19 revenue, as shown. Note that approximately 43.9% of wafer sales revenue was reported for process nodes larger than 65 nm, which is therefore not represented in the table below. The state of use is summarized below and defined based on market share and on the variety of current-generation chipsets using technology based at that node. Table 7 also provides examples of the chipsets typically manufactured at a given node for additional context.

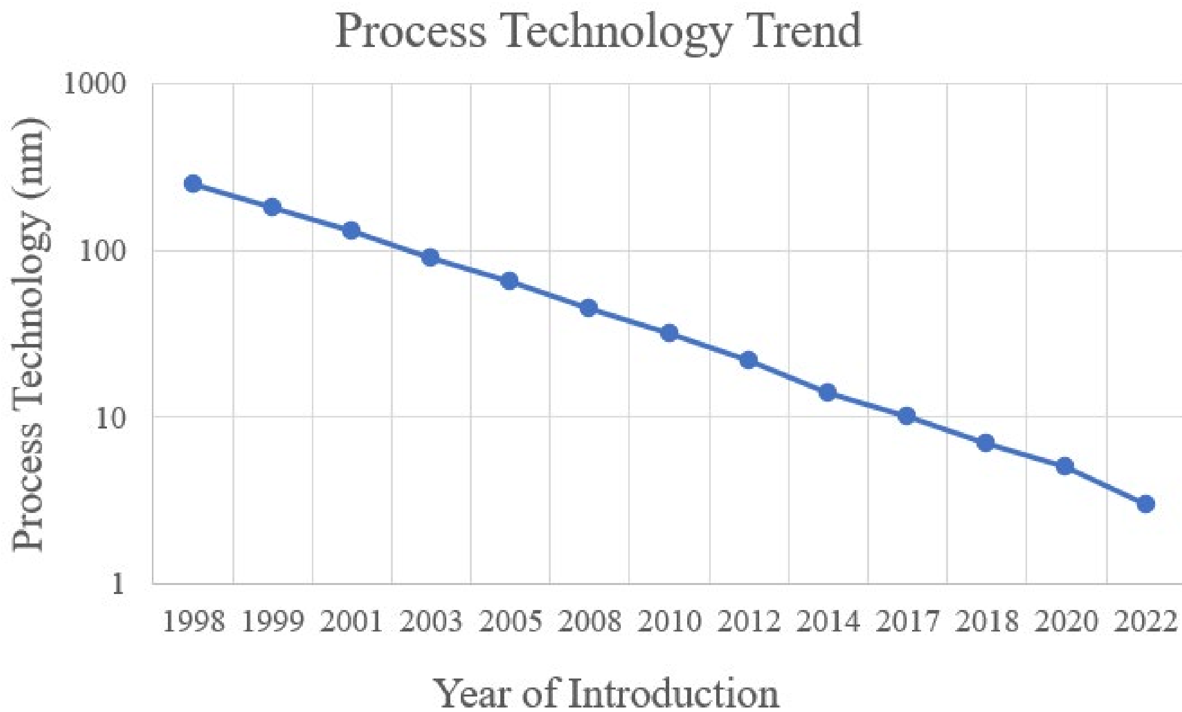


Figure 26: Process technology vs. year of introduction [85].

Table 7: Current state of the art of process nodes or technologies [86], [87].

65 nm	Market Penetration: 22.6 %
Maturity:	High. Introduced in 2005. United Microelectronics Corporation (UMC) developing specialty technology at this node in 2019.
Use:	High. Used in relatively low-computing power and non-space constrained applications such as computer and server processors, and digital cameras.
40/45 nm	Market Penetration: 15.4 %
Maturity:	High. Introduced in 2007. UMC was developing specialty technology at this node in 2019.
Use:	High. Used in automotive processors, image processing, personal computers and servers, and low-power chipsets.
28 nm	Market Penetration: 6.7 %
Maturity:	High to Moderate. Introduced in 2011. UMC is working on process improvement research for production in 2021. Samsung was developing SoC at this node for production in 2019.
Use:	Moderate. Used in entry-level smartphones and workstations, advanced SoC designs, desktop computers and some machine learning chipset architectures.
20 nm	Market Penetration: 0.2 %
Maturity:	Moderate. Introduced in 2014. UMC developing process improvements for implementation in 2020.
Use:	Low. Intermediate process node used by some inexpensive smartphones and specialty computing hardware.
16 nm	Market Penetration: 4.5 %
Maturity:	Moderate. Introduced in 2014. Semiconductor Manufacturing International Company (SMIC) completed initial research and development in 2019 to begin large-scale production [2]. UMC completed product assessment in 2019 to begin risk production in 2020.
Use:	Moderate. Current generation of laptops and desktop processors, high-performance smartphones, supercomputer processors, graphics processing

	units, computer vision chipsets, random access memory controllers.
10 nm	Market Penetration: 0.6 %
Maturity:	Low. Introduced in 2016. Samsung was developing DRAM and processor technology at this node in 2017 & 2018.
Use:	Low. Applications are similar to those at the 16 nm node, but manufacturing is not yet fully mature. The industry is scheduling the production of high-end smartphones implementing this technology in 2021.
7 nm	Market Penetration: 6.1 %
Maturity:	Low. Introduced in 2018. SMIC research and development focused on developing 7 and 5 nm large-scale production implementations. Samsung was researching new 7 nm lithography processes in 2018 and planning to use some 7 nm chipsets in the Galaxy Note 10 in 2019.
Use:	Low. Supercomputer processors, neural network processing, high-end smartphones, graphics processing units, and personal computers. Applications in development for production 2021-2022.

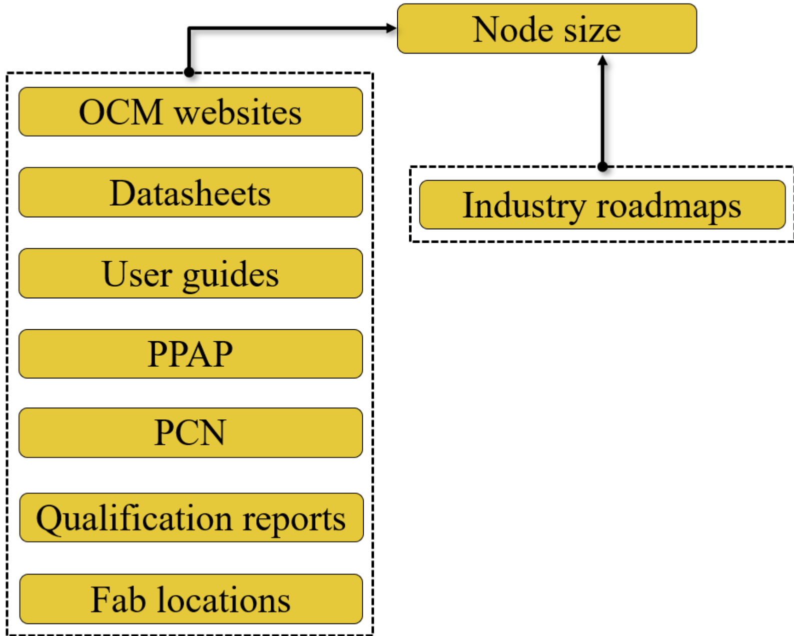


Figure 27: Documents through which part manufacturers can report process technology.

Overall, obtaining the process technology of the active electronic component is challenging but not impossible. It is possible to obtain part process technology based on the assessment of the information provided by the original part manufacturer. In addition, engineering judgment can be made based on the year of introduction, part type, and roadmaps developed by the industry (e.g., ITRS, IMEC). Based on the active integrated circuit (IC) parts used for reliability assessment, a procedure to obtain the process technology through various manufacturer-provided documents is developed, as shown in Figure 27. These documents can be used as a starting point to obtain process technology, which can be extended further if needed.

3.4. Methodology to Obtain Process Technology

The following steps, as shown in Figure 28, outline a systematic approach for obtaining process technology information from part manufacturer documents. The first step involves collecting relevant documents such as datasheets, qualification reports, reliability reports, PCNs, and PPAPs, as discussed in Section 3.3. These documents should specifically pertain to the desired part, and the very first source of information or identifying part-related documents is the part manufacturer's website or webpage.

Subsequently, thoroughly review the collected documents to identify any explicit or implicit information related to the process technology. Cross-referencing the information obtained from different documents is crucial to identify consistencies and discrepancies. It helps validate the accuracy and completeness of the obtained information. Validating the document is vital when the identified document is related to the part being purchased. It is essential to ensure that the information provided in the datasheet accurately represents the specifications and characteristics of the part. Figure 29 provides a procedure to validate the datasheet.

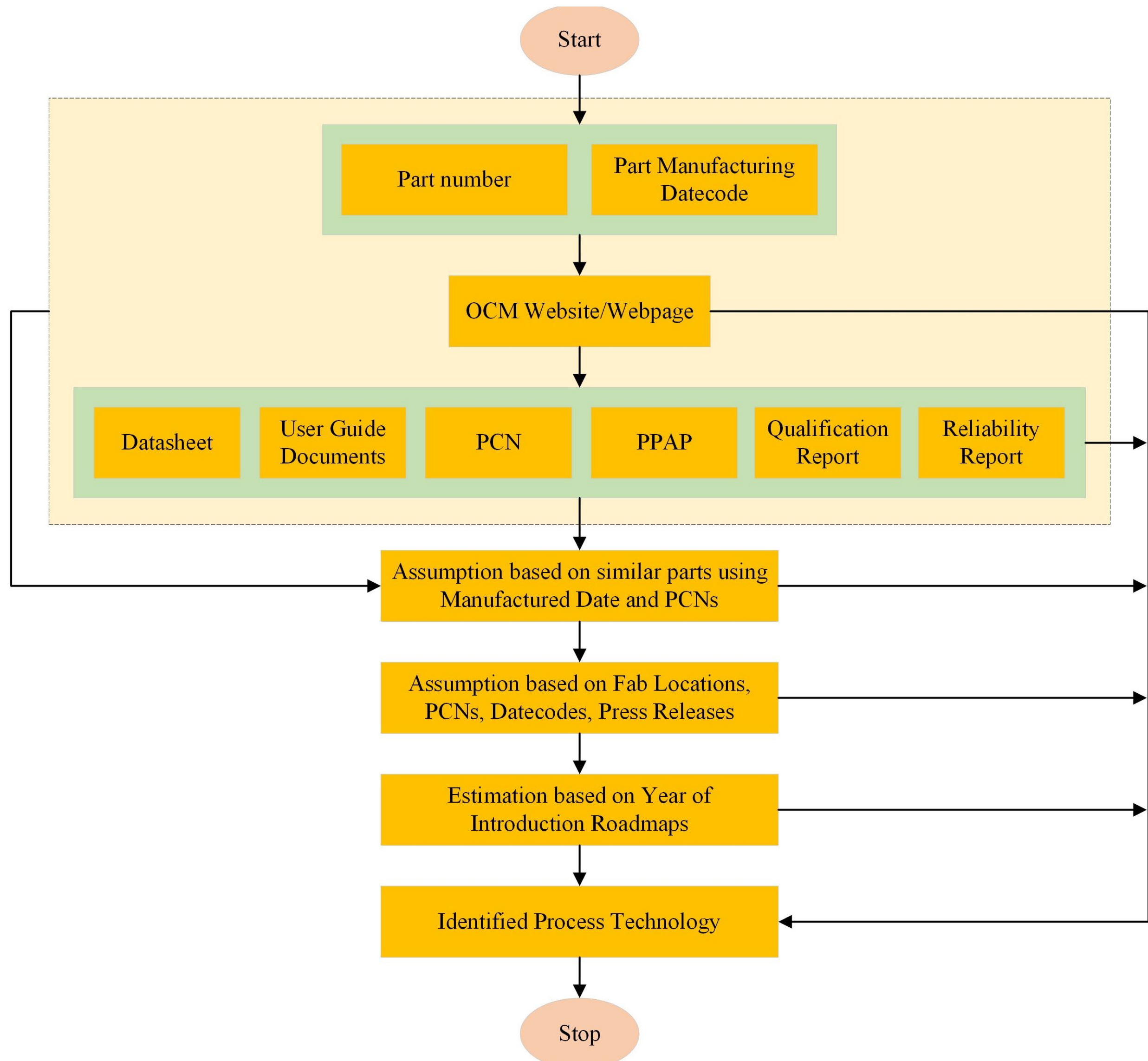


Figure 28: Methodology to obtain part process technology.

Formulation of assumptions is vital when specific process technology information is not explicitly mentioned in the part manufacturer documents. These assumptions are based on similar functional parts or components fabricated by the same manufacturer or within the same fab location. Industry knowledge, technological trends, and experience are valuable inputs for formulating reasonable assumptions regarding the process technology parameters.

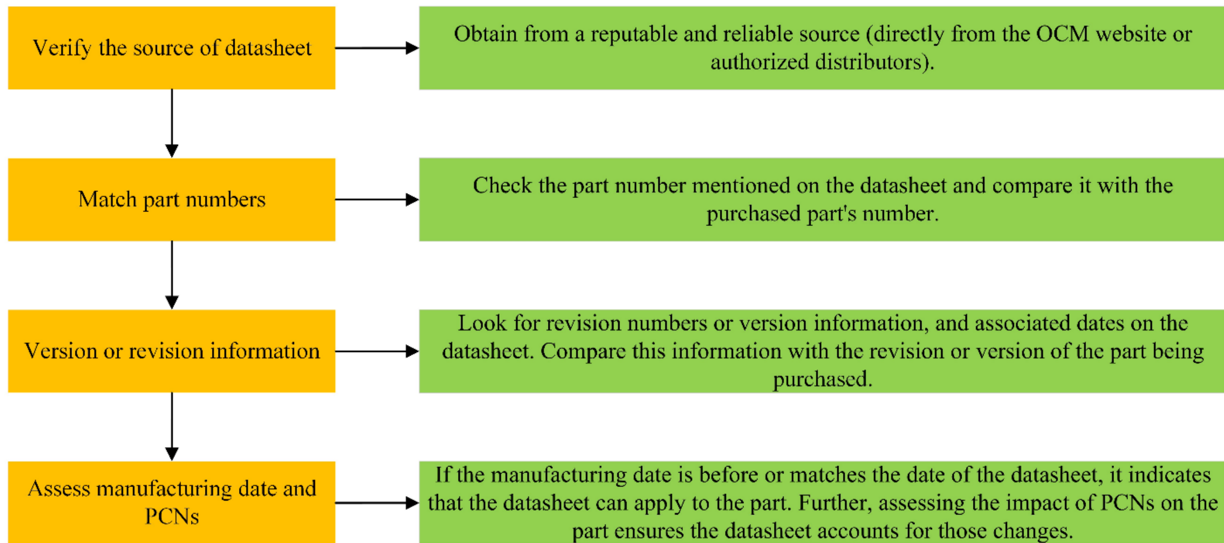


Figure 29: Example of procedure to validate datasheet.

In addition to the previously mentioned steps, further assumptions can be made based on additional factors such as the fab location, PCNs, date codes, and press releases provided by the manufacturer. The fab location can play a significant role in determining the process technology employed. Different fabs may have specific capabilities or expertise, and understanding the site can provide insights into the likely process technologies used. PCN notifications can sometimes reveal information related to process technology modifications. Press releases or public announcements by the manufacturer can also be valuable sources of information. Manufacturers often share updates about process technology advancements, collaborations, or new manufacturing capabilities. Monitoring such announcements can provide helpful context and indications of the process technology employed by the manufacturer. By considering these additional factors, researchers can make informed assumptions while estimating process technology. While these assumptions may not provide direct or explicit process technology information, they serve as process technology estimation.

Consulting industry-developed roadmaps, such as technology nodes or industry standards, is another essential step in the methodology. These roadmaps provide a general understanding of process technology advancements and can guide the estimation process. The process technology estimation is achievable by leveraging the year of introduction or the fabrication timeline of the part.

There are various sources of information to obtain part process technology, but identifying the best source depends on the risk associated with the document and the assumptions. Figure 30 provides the sources of information from the low to high risk, which can affect the accuracy of the obtained process technology. For example, identifying the process technology through the part website has low risk as the information on the part manufacturer's website is the most reliable source. Similarly, process technology estimated through roadmaps is of greater risk because the estimated process technology might not be the exact process technology the part is manufactured with.

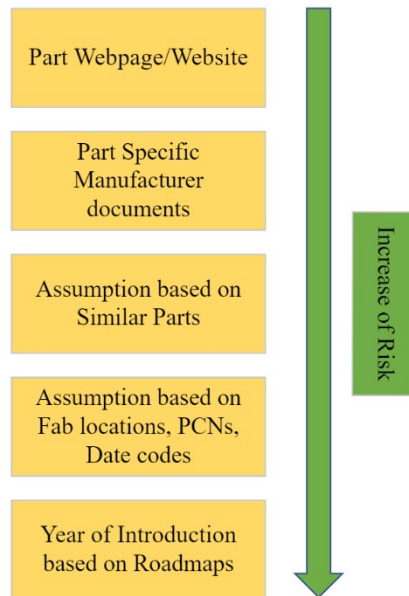


Figure 30: Increment of risk associated with the information source of a part process technology.

4. Part Reliability Assessment and Management Methodology

The project is developing a methodology to assist a user in assessing active electronic parts' reliability at die-level failure mechanisms based on life cycle environmental conditions, operating conditions, and part architecture. This work will act as an approach for ultimately identifying the parts for the application that maximize part reliability with minimized implementation and testing costs.

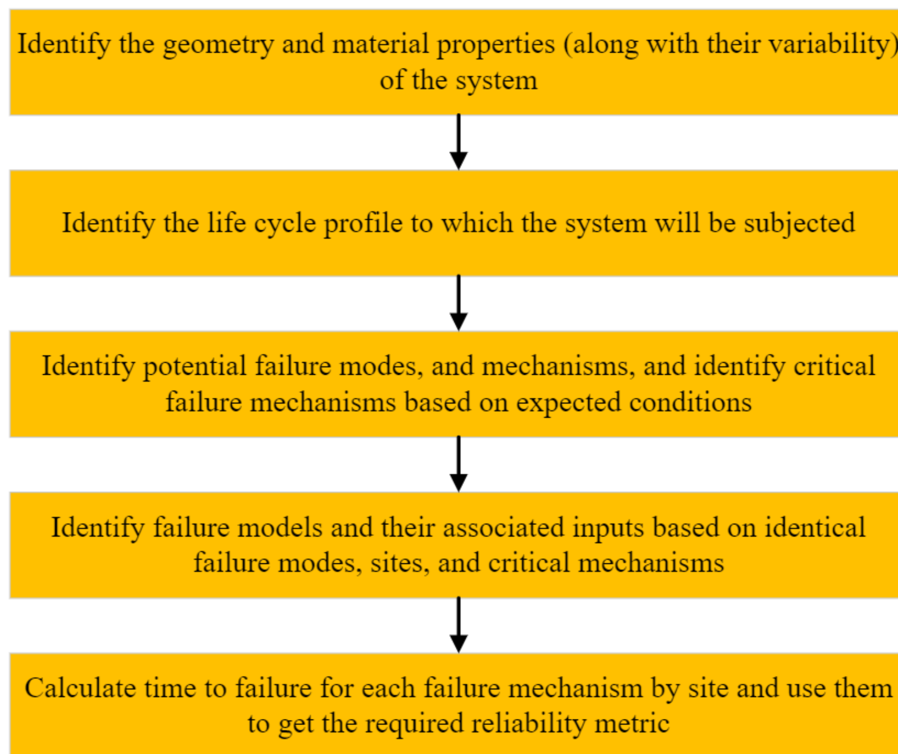


Figure 31: Process for completing stress and damage modeling for reliability prediction [88].

The workflow in Figure 31 is an application of IEEE Standard 1413 section 5.4.1 [88], which states the process for completing stress and damage modeling for reliability prediction. This process says that for a given system, the first step is to identify the geometry, material properties, and variability of these properties intrinsic to the system. With this in mind, the next

step is to estimate and identify a life cycle profile or a series of profiles to which the system will be subjected. The next objective is to use failure modes, mechanisms, and effects analysis to identify potential failure sites and critical failure mechanisms based on the system properties and application conditions. Using the results of FMMEA, the next step is to identify the specific failure models needed and then ultimately calculate different reliability metrics, such as time to failure and other metrics.

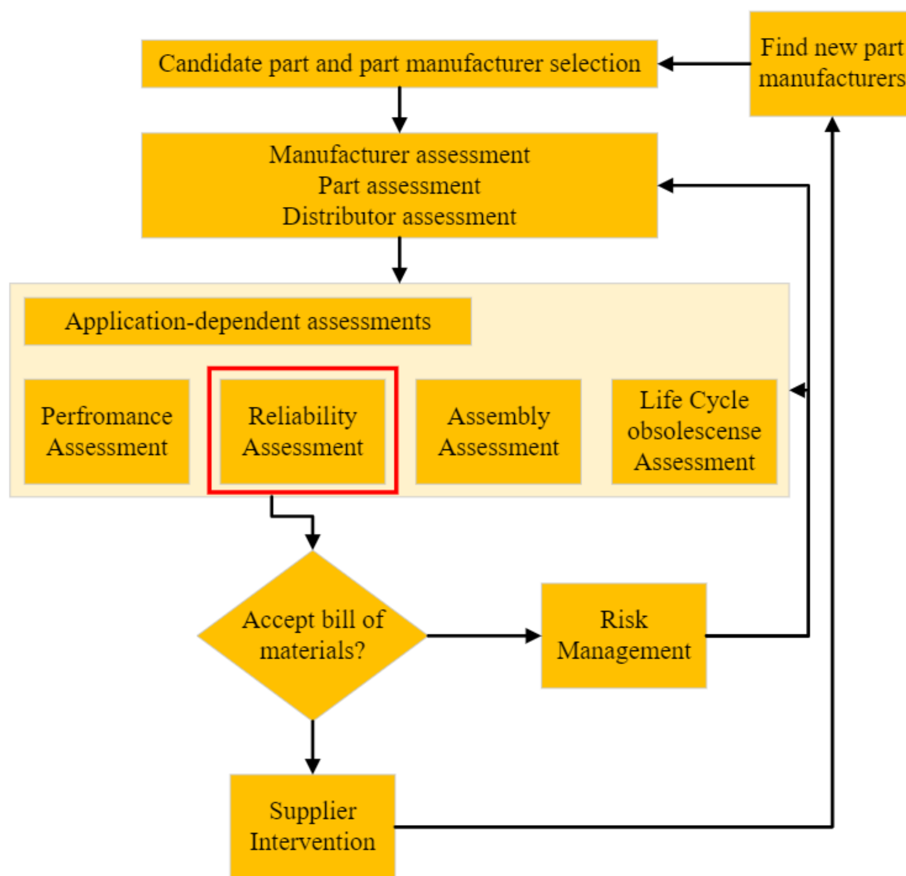


Figure 32: Part selection and management developed by CALCE [89].

This work is a continuation of focused-on application-dependent reliability assessment criteria of risk-informed methodology for electronic part selection and management developed by CALCE [89]. Parts selection and management is a process designed to evaluate the risks

inherent in using an electronic part and then facilitate informed decisions regarding its selection and future management activities. This process aids in determining the acceptability of a part for an application while considering factors such as functionality, performance, standardization, cost, availability, technology (new and aging), and logistics support. It includes application-independent (availability, cost, manufacturer, distributor, and part quality and integrity assessments) and application-dependent (determination of the local environment and performance, reliability, assembly, and life cycle obsolescence assessment) considerations. This project focuses on reliability assessment criteria of part management methodology (shown in red block) as shown in Figure 32 [22].

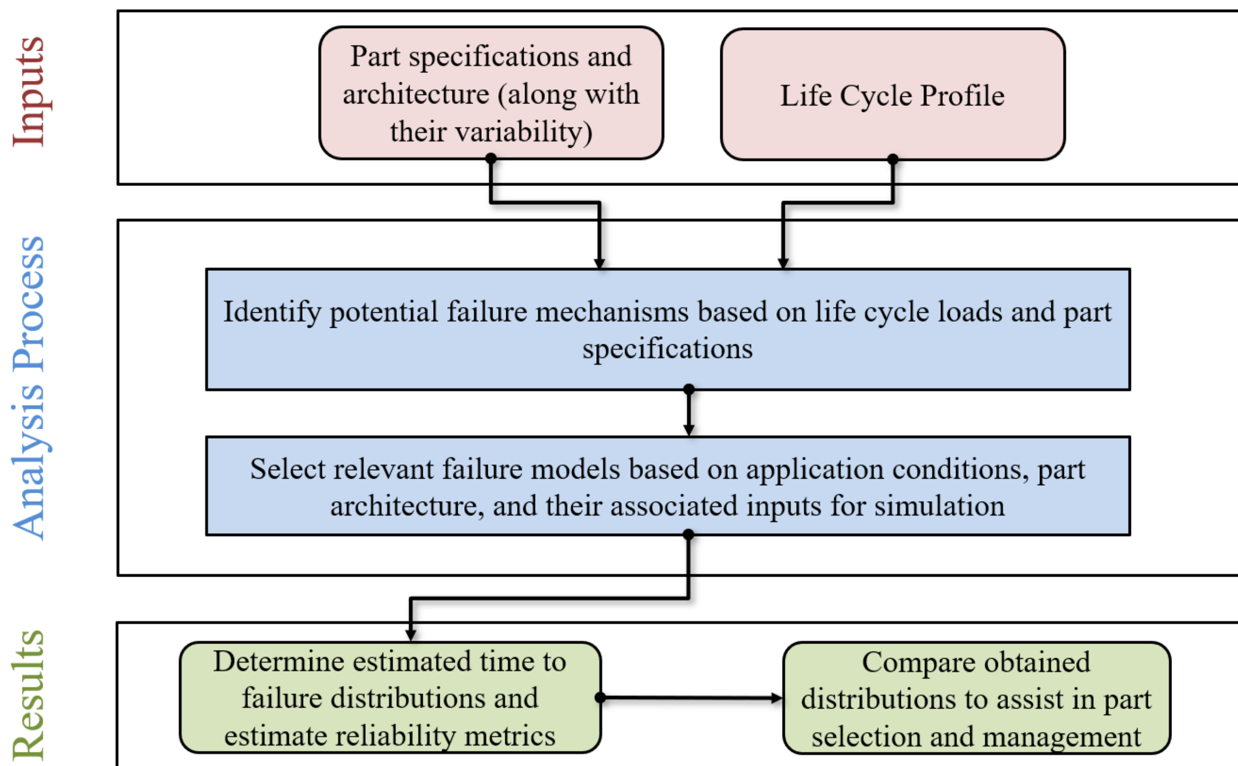


Figure 33: Part reliability assessment and selection methodology [22].

Before conducting the part's reliability assessment, the user must perform a manufacturer, part, and distributor assessment for a candidate part based on part selection and management

methodology. Deconstructing the workflow in Figure 31, without accounting for experimentation costs to identify unknown model parameters, Figure 33 shows the workflow to conduct part reliability assessment and selection process to ensure that part will function within a specific life cycle [22]. It details the inputs and analysis process needed for garnering reliability information (e.g., time to failure (TTF) distributions, uncertainty distributions).

This methodology can assist users in selecting a candidate part among various alternative parts and manufacturers, replacing parts based on different packaging types or application conditions, or estimating the reliability of parts with technology levels for future selection. This approach for identifying the parts for an application maximizes part reliability with minimized implementation and testing costs. Several types of information are required to estimate the time to failure for different application conditions and to analyze the uncertainty of product survival. This methodology grouped types of information required to conduct physics of failure-based time-to-failure simulations into two types, as shown below,

- Information about part specifications and architecture
- Information about failure mechanisms and models

A methodology is developed to obtain a part-life estimation, as shown in Figure 34. The process is illustrated using the TDDB failure mechanism as an example. The procedure begins with the part and the failure mechanism TDDB in the provided example. Based on the literature and data collection process performed for the part, select a failure model or TTF equation that best correlates with the TDDB failure mechanism. For the chosen failure mechanism, identify the input parameters, such as part specifications, architecture, and model constants, into the TTF equation. These parameters have the option to plug in as distributions are limited to uniform and normal. Performing all these steps provides results that can be obtained as TTF or log (TTF)

distribution estimates, which can also be interpreted as B_x life. For n different types of parts, this methodology can be repeated, and the results can be compared to rank the parts based on the life estimates for the TDDB failure mechanism, which assists in selecting parts based on reliability requirements.

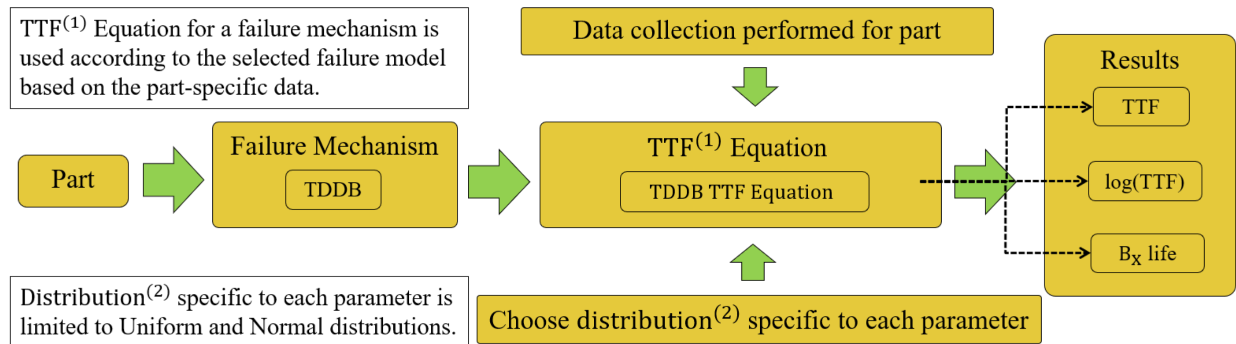


Figure 34: Part-life estimation methodology for a failure mechanism (TDDB).

Based on the failure modes, mechanisms, effects, and analysis (FMMEA), the methodology mentioned above can be extended further to other critical failure mechanisms such as HCI, EM, and NBTI, as shown in Figure 35.

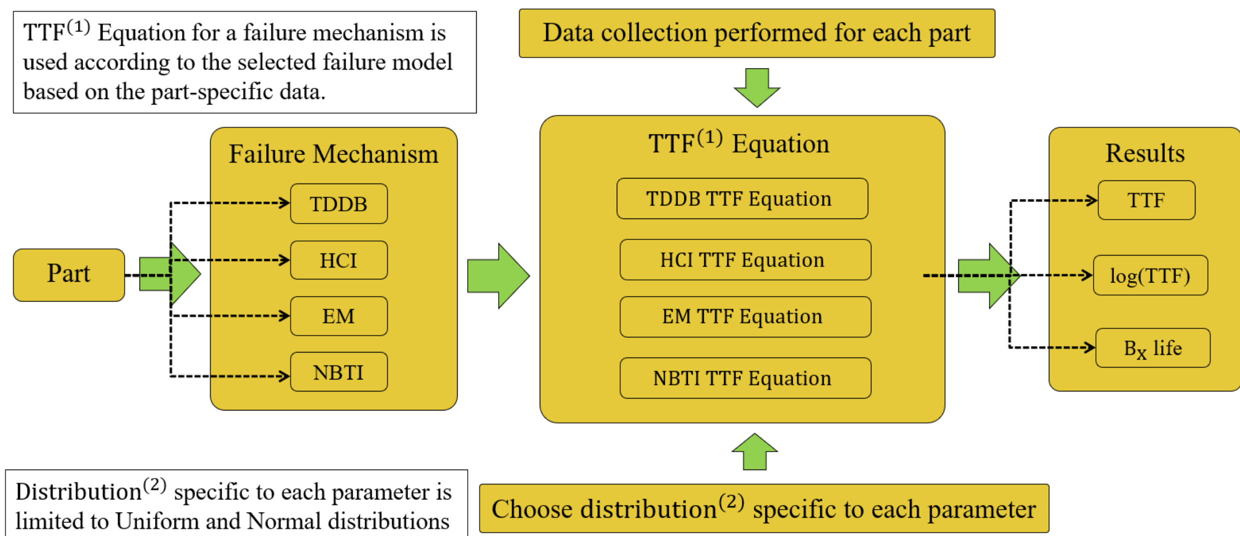


Figure 35: Part-life estimation methodology extended to four die-level failure mechanisms.

Literature, standards, and part-associated documents will be assessed as shown in Chapters 1, 2, and 3 to obtain part parameters and failure model information. Once the user gets information on the estimated application use conditions, part specifications for each part, and model constants for each part corresponding to the different failure models, which is discussed in Chapter 5, all this information is then used to evaluate other failure mechanisms to identify the most critical of them. This project is limited to assessing parts based on four die-level failure mechanisms, which are time-dependent dielectric breakdown (TDDB), hot-carrier injection (HCI), electromigration (EM), and negative-bias temperature instability (NBTI). Next, the input application conditions, part specifications, and modeling information is plugged into the failure models corresponding to the most critical failure mechanisms and using these failure models, the next step is calculating and evaluating the desired reliability information and selecting the reliable part based on the time-to-failure distribution as described in Chapter 6.

5. Obtaining Input Parameter Information of Failure Models, Simulation, and Results

Reliability estimation is critical to assessing the performance and durability of electronic components and systems [90]. It is essential to have reliable input parameter information for the chosen failure models to estimate reliability accurately [91]. This chapter focuses on obtaining input parameter information for failure models of die-level failure mechanisms (EM, TDDB, and HCI) mentioned in Chapter 2. It also addresses the challenges of acquiring accurate input parameters by identifying the relevant failure models for the specific electronic parts under consideration.

The procedure begins with identifying the critical die-level failure mechanisms for the parts of interest to perform selection amongst them. For these failure mechanisms, obtain the failure models available through the literature. Since this thesis aims to perform part selection without any testing, we utilize part-related documents through various sources of information listed in Table 6 to identify the model parameters. Through these sources, the first parameter to identify is the process technology of a part. The methodology to obtain the part process technology is illustrated in Chapter 3. The main reason for identifying the part process technology is to select an appropriate failure model based on part-specific conditions. It also provides details of other model parameters, such as gate oxide thickness and metal interconnect width. Once the process technology has been identified and the failure model is selected based on part-specific information, the inputs in the model equation can be classified into three categories: model constants, geometric parameters, and application conditions.

5.1. Parameter Information of Failure Models

An electronic part's reliability depends on application conditions, part information, and modeling constants [92]. Information related to these factors must be found (or approximated) for a proper reliability estimation to be made. As each input is treated as a distribution representing information uncertainty, the more information that can be found, the less uncertain the final time to failure distribution will be [93]. Each of the three main input aspects is discussed below in the context of methods of collecting information and quantifying the uncertainty in the information.

5.1.1. Model Constants

Model constants consist of all the parameters of the failure models of EM, TDDB, and HCI that are independent of the part. Extensive research has been completed on various parts to determine model constants that accurately project the time to failure. Using this information, ranges on the modeling constants have been developed and summarized. The ranges and modeling constants for three semiconductor wear-out failure mechanisms and associated models are presented in Table 8 [23].

Table 8: Model constants of three die-level failure mechanisms and associated models [23].

Model Constant	Value or Range
EM: A_0	Assumed as constant or 1
TDDB: B_0	Assumed as constant or 1
HCI: C_0	Assumed as constant or 1
EM: E_{aa}	Al: 0.6 eV Cu: 0.9 eV

Model Constant	Value or Range
TDDB: E_a	2 eV
HCI: E_{aa}	In eV For N − channel: 0.3 For P − channel: (L > 0.25μm): −0.15 (L < 0.25μm): 0.25
EM: n	Al: 2 Cu: 1.1
HCI: n	3
TDDB: γ	$\frac{1508}{T}$ cm/MV
TDDB: G(T)	350 MV/cm
TDDB: τ_0(T)	1 x 10^{-11} s
k	8.62 x 10^{-5} eV/k

According to JEP122H, model constants provided in the standard are the values identified based on years of research and experimental data to estimate these parameters. A_0, B_0, and C_0 are the scale factor values of the three failure mechanisms models EM, TDDB, and HCI. These factors typically vary from part to part, due to which a distribution is obtained for the estimated time to failure [23], [35]. However, to identify this value, one must perform testing, which is not an option for die-level failure mechanisms as they may take from 10 to 100 or 1000 years [94]. These model constantly change based on process technology.

Additionally, literature lacks an adequate number of sources that provide a scale factor to estimate based on the articles available in IEEE since 1989 – 2022, as each mechanism has around 250 publications and little to no information is available for scale factor [95]. Therefore,

these values are estimated as constant for all the parts to estimate TTF as they only scale the TTF distributions. The only drawback is that the estimated TTF distributions are not accurate but scaled to different values. Though these distributions cannot be used for expressing the time to failure, one can use them to rank different parts.

Activation energy is a critical parameter in understanding and predicting failure mechanisms in integrated circuits. It represents the energy barrier that must be overcome for a specific failure mechanism to occur. It is typically measured in electron volts (eV) and provides insights into the reliability and lifetime of electronic devices. The activation energy in EM reflects the energy required for atomic diffusion within the metal and is predominantly dependent on the metal. Metal interconnects are made with Aluminum, Copper, and a few other alloys. For aluminum, the activation energy is about 0.6 eV, and 0.9 eV for copper. The activation energy in TDDB represents the energy required for the breakdown process, such as electron tunneling or defect generation, impacting the reliability and lifetime of the dielectric. The activation energy required to break the Si-O bond is 2 eV. Due to the effect of temperature, the amount of activation energy required to break the bond is less than 2 eV. The amount of reduction is calculated by the gamma parameter, which is 1508/T cm/MV. HCI is a failure mechanism that affects both n-channel and p-channels. It occurs when high electric fields near the drain or source regions cause energetic electron or hole injection into the gate oxide. This injection introduces trapped charges and oxide degradation, leading to threshold voltage shifts and device performance degradation. The activation energy in HCI reflects the energy barrier for charge injection. For n-channel, the activation is approximately 0.3 eV. For p-channel, if the channel length is greater than 0.25 μm, the activation energy is -0.15 eV, and 0.25 eV if greater than 0.25 μm.

The other model parameter which affects the time-to-failure values exponentially is the n constant. The value of the n for the EM varies based on the material used. For aluminum, the n value is 2, and for copper, it is about 1.1. The n value also lies in HCI, whose value is about 3. The other parameters, such as G(T) and $\tau_0(T)$, are also provided in the JEP122H standard, and their values are 350 MV/cm and 1×10^{-11} s. The final model constant used in all failure models is Boltzmann's constant, 8.62×10^{-5} eV/k.

5.1.2. Geometric Parameters

The geometric parameters refer to the characteristics and properties of the parts' shape, size, and spatial configuration. These parameters influence the reliability and failure mechanisms observed in integrated circuits. The part selection based on estimated time-to-failure distributions is demonstrated through three CMOS parts whose part numbers are SN74LV244ADWR, SiT2024BM-S2-33E-40.00E, and A3PE3000-2PQG208I. The process technology of these parts is identified through the methodology mentioned in Chapter 3. Based on the process technology and part-specific documents, geometric parameters required for EM, TDDB, and HCI are identified, as shown in Table 9.

Table 9: Geometric parameters of three die-level failure mechanisms and associated models.

Geometric Parameters	**CMOS Part Name (Process Technology)**		
	SN74LV244ADWR or P1 (1.2 µm)	**SiT2024BM-S2-33E-40.00E or P2 (0.18 µm)**	**A3PE3000-2PQG208I or P3 (0.13 µm)**
EM: Interconnect width	1.2 µm (Cu) [73]	0.306 µm (Cu)	0.28 µm (Cu) [96]
TDDB: Gate oxide thickness	22.5 nm [73]	3.2 nm [97]	5.2 nm [98]
HCI: Gate channel length	1.1 µm [73]	0.13 µm	0.22 µm [98]

Based on the failure models, the required geometric parameters are metal interconnect width, gate oxide thickness, and gate channel length. The width and height of the metal interconnect impact the current density distribution within them. Narrow or tall interconnects experience higher current densities, increasing the susceptibility to EM-induced failures. In CMOS, interconnect thickness is considered negligible when compared with interconnect width, due to which it is approximated to be a constant considered into scale factor. The thickness of the gate oxide influences the electric field strength at the metal-oxide interface. Thinner gate oxides exacerbate the impact of HCI due to enhanced electric fields and higher injection energies.

Additionally, gate oxide thickness assists in selecting a failure model for TDDB and is also an input parameter for the E model. In CMOS, the channel length and width affect the electric field distribution. Smaller channel lengths and narrower widths intensify the electric fields near the drain or source regions, promoting HCI-induced degradation. The channel length is also a selection parameter for the HCI failure model. These parameters are identified for the three parts from various sources of information.

5.1.3. Application Conditions

Application conditions are the last set of parameters required for modeling time to failure estimates. Five application conditions are required as parameter inputs for all the models: current, temperature, gate voltage, peak substrate, and gate current, as shown in Table 10 [23]. A set of application conditions based on user requirements is to be provided. One can select a part by comparing the parts of interest at these application conditions.

Table 10: Application conditions of three die-level failure mechanisms and associated models.

Application Conditions	Value or Range

Application Conditions	Value or Range
Current	50 mA
Temperature	50°C or 323K
Gate voltage	3.5 V
HCI: Peak Substrate Current	1 µA
HCI: Peak Gate Current	1 µA

5.2. Simulation and Analysis

To obtain the time-to-failure estimates of all the failure mechanisms for the parts mentioned in the previous section, one can obtain them numerically by plugging in the parameter values. The efficient way to code the failure models is such that one can plug in the parameters and obtain the time-to-failure estimates instantly. Since this process needs to be performed for all three failure mechanisms and their respective failure models for each part would consume a lot of time, a graphical user interface (GUI) is developed in MATLAB to access the whole process as an application for customer friendly interface. The GUI begins with a window consisting of the list of the three failure mechanisms and a start button, as shown in Figure 36. When one of the failure mechanisms is clicked, and then the start button, a new window concerning the failure mechanism selected will pop up.

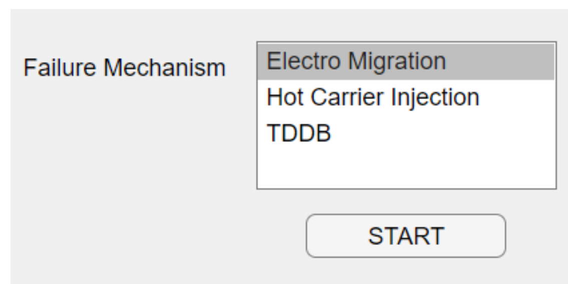


Figure 36: GUI initial window.

The pop-up window changes for each failure mechanism. For electromigration (EM), the window is shown in Figure 37. It consists of all three sections of parameter inputs to estimate the time-to-failure distribution. Apart from the parameters, there is an option to choose the type of distribution applied for all the parameters consisting of normal and uniform distributions. For the normal distribution, the first block is the mean, and the second block is the standard deviation. For uniform distribution, the first block is the lower limit, and the second block is the upper limit. Plug in the values obtained in Section 5.1 concerning the part.

Figure 37: GUI window for electromigration.

Similarly, the TDDB also has a separate window, but the type of failure model separates it. For the E model, the GUI is shown in Figure 38, and for the 1/E model, the GUI is shown in Figure 39. The HCI window is shown in Figure 40, which consists of all the aspects concerning the model selection based on channel type and length. The values plugged in the windows' figures are for part SN74LV244ADWR and of the standard deviation of 12 percent of the mean value.

Data Input | Analysis | Datasheets | +

Current Failure Mechanism: TDDB E Model

Parameter Distribution

Distribution

Normal

Uniform

User Input

Gate Voltage (V) 3.5 to 0.07

User defined temperature (C) 50 to 1

Model Parameters

Scale parameter (Time Units) 1 to 0.02

Activation Energy (eV) 2 to 0.04

Field Acceleration (cm/MV) 4.669 to 0.093

Part Specfications

Gate oxide thickness (nm) 22.5 to 0.45

Figure 38: GUI window for TDDB E model.

Data Input | Analysis | Datasheets | +

Current Failure Mechanism: TDDB 1/E Model

Parameter Distribution

Distribution

Normal

Uniform

User Input

Gate Voltage (V) 3.5 to 0.07

Model Parameters

Scale parameter (Time Units) 1e-11 to 3.3e-07

Field Acceleration (cm/MV) 350 to 7

Part Specfications

Gate oxide thickness (nm) 22.5 to 0.45

Figure 39: GUI window for TDDB 1/E model.

Figure 40: GUI window for HCI failure models.

Once all the parameter values are plugged-in, click on the analysis tab next to the current data input tab. The analysis tab consists of a plot with axes labeled CDF (cumulative distribution function) and TTF (time to failure), as shown in Figure 41. The plot auto-scales to the distribution plotted onto it. When the calculate button is clicked, it plots the TTF distribution based on the parameter values plugged in the data input tab. The GUI allows the plotting of multiple TTF distributions onto the same axes for comparison. We can obtain this by returning to

the data input tab, plugging in new parameters, and clicking calculate in the analysis tab again. Now, we will have two TTF distributions plotted onto the same axes available for comparison based on the parameters provided. The clear button clears all the plotted distributions at once. It also provides the B_x life or time-to-failure at x percent of CDF when the x value is provided.

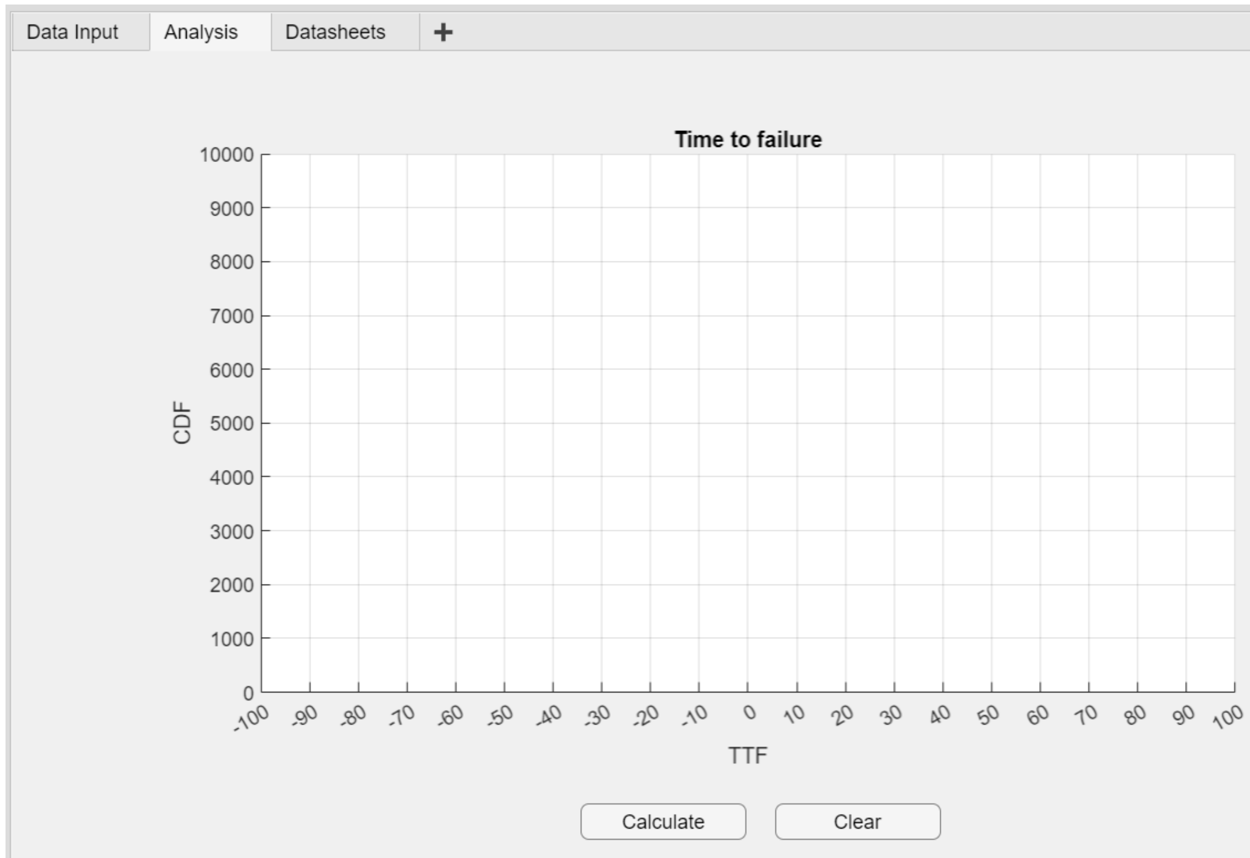


Figure 41: Analysis tab to view the TTF distribution plotted based on the parameters provided in the data input tab.

Often in industries, the part-related information is not collected properly. Even if they collect the information, storing it is critical. The GUI consists of an option to store the information for a part and retrieve it whenever required through the datasheets tab, as shown in Figure 42. The analysis tab and the datasheets tab consist of similar layouts due to which the figures provided are of electromigration window, but they are applicable for TDDB and HCI.

Data Input | Analysis | Datasheets | +

Component Datasheet

Component: SN74LV Series / Item 2 / Item 3 / Item 4

Show

Information for Failure Model		Electromigration		
Failure Model Attribute	Details	Units	Source	Assumption
Arbitrary Scale Factor	1	Arbitrary unit	Scale factor can be obtained from literature having the same architecture and material or estimating factor from experimental results	No information obtained from literature review about the scale factor for component architecture and material so it is assumed to be 1
Metal I or II pitch (width/space)	1.2	µm	Referred from MITEL Semiconductor, 1.2 µm CMOS process family, April 1998	Metal I or II pitch dimensions are used for study as they are
Cross-sectional area of interconnect	1.2*0.8	µm^2	Assuming 0.8 as aspect ratio	
Metallization Material	Copper		Referred from Material Declaration document	
Current Density	Calculated based on maximum current (mA) through Vcc or GND obtained from datasheet and cross-sectional area of interconnect (µm^2)	mA/µm^2		
Activation energy	0.85 to 0.95	eV	C.Christiansen, F.Chen, M.Angyal, T.Bolom, E.Kaltalioglu "Reliability Challenges in Copper Metallizations arising with the PVD Resputter Liner Engineering for 65 nm and beyond," IEEE International Reliability Physics Symposium Proceeding,s 2007, pp. 511-515	
Current Density Exponent	1.1 to 2	Constant	C.Christiansen, F.Chen, M.Angyal, T.Bolom, E.Kaltalioglu "Reliability Challenges in Copper Metallizations arising with the PVD Resputter Liner Engineering for 65 nm and beyond," IEEE International Reliability Physics Symposium Proceeding,s 2007, pp. 511-515	
Junction Temperature	Calculated based on junction to ambient thermal resistance of package, power dissipation, and ambient temperature			

Figure 42: GUI datasheets window to access previously stored part-related information.

5.3. Simulation Results

The simulation results of time-to-failure estimations are obtained for the three parts mentioned in previous sections. Using the B_x life, a comparison between the parts is performed to either select or rank the parts accordingly. The simulations are performed at two conditions for the same parameter inputs, except the deviations are varied to quantify the impact of error in part identified parameter. For this, the simulations are run at 1 percent and 2 percent deviation ranges, and the results are as follows. The results are shown for all three parts with respect to the failure mechanism. The Monte Carlo technique estimates the TTF distributions of the failure mechanisms. The Monte Carlo method is a type of computational algorithm that uses the process of repeated random sampling for parameters for various numerical estimations and

simulation purposes [99]. One should identify the number of random samplings used to generate the estimates. Smaller samplings may not be saturated or provide inaccurate results, and a higher number provides overestimation or time complexity issues. It can be resolved by running the GUI at various instances ranging from 100 to 10000. The results obtained at 1, 10, and 50 percent life are consistent and saturated, as shown in Table 11 when simulated for EM at the 2 percent deviation range.

Table 11: Variation of estimated TTF at different numbers of random sampling.

Number of Random Generated Instances	**B_x Life (x1E+08)**		
	X = 1 Percent	**X = 10 Percent**	**X = 50 Percent**
100	6.8535	7.7468	9.013
1000	6.8535	7.7443	8.9956
3000	6.8454	7.735	8.9872
6000	6.8419	7.7341	8.9854
10000	6.842	7.733	8.984

The B_x Life is obtained from the cumulative distribution function (CDF) plots produced based on the histogram modeled using the TTF failure models. The CDF vs. TTF plot of EM at 1% parameter deviation range for P1 is shown in Figure 43. Based on the obtained plots, the GUI produces the B_x Life estimates by interpolating when provided with the required or interested x value. Hence, a similar procedure is used to obtain the results at three different x values. The results are provided in Tables 12, 13, and 14 for EM, TDDB, and HCI as B_x Life at 1, 10, and 50 percent with 1 and 2 percent parameter deviation range for the three parts P1, P2, and P3.

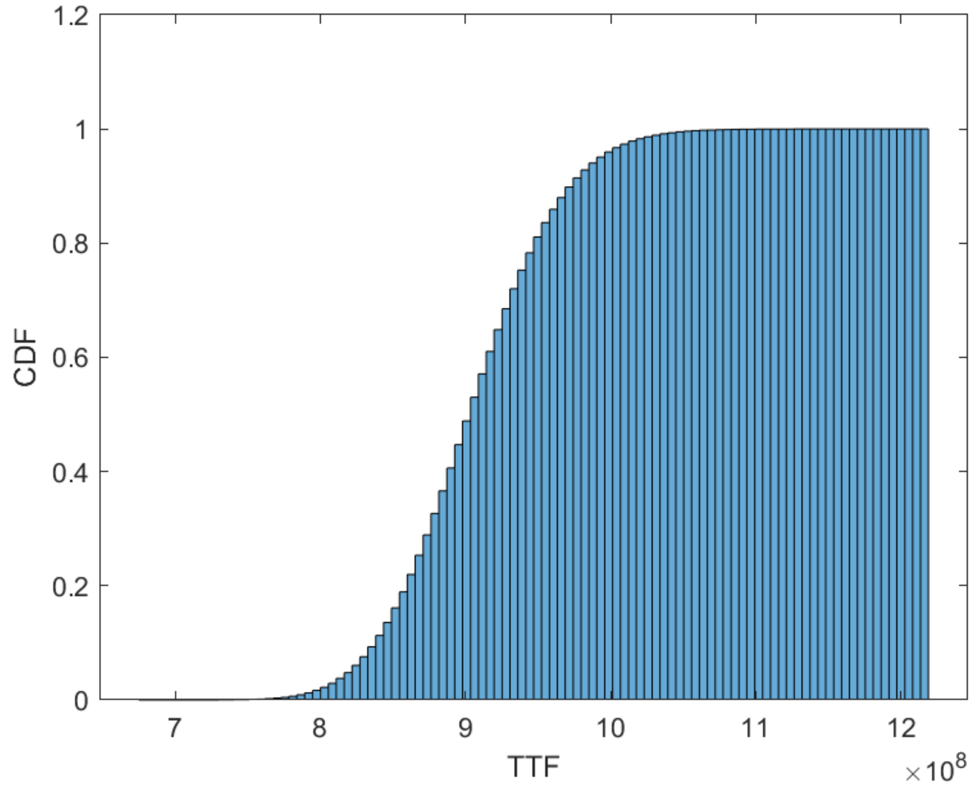


Figure 43: CDF Vs. TTF for EM at 1% parameter deviation range of P1.

Table 12: Results of EM as B_x Life.

EM B_x Life Estimates for P1, P2, and P3		**1% Parameter Deviation Range**	**2% Parameter Deviation Range**
P1	**B_x Life at 1%**	7.8809E+08	6.8518E+08
	B_x Life at 10%	8.3739E+08	7.7447E+08
	B_x Life at 50%	9.0225E+08	8.9964E+08
P2	**B_x Life at 1%**	1.7489E+08	1.5174E+08
	B_x Life at 10%	1.8608E+08	1.7184E+08
	B_x Life at 50%	2.0071E+08	2.0006E+08
P3	**B_x Life at 1%**	1.5854E+08	1.3773E+08

EM B_x Life Estimates for P1, P2, and P3		1% Parameter Deviation Range	2% Parameter Deviation Range
	B_x Life at 10%	1.6872E+08	1.5581E+08
	B_x Life at 50%	1.8202E+08	1.8147E+08

Table 13: Results of TDDB concerning the failure model as B_x Life.

TDDB B_x Life Estimates for P1, P2, and P3		1% Parameter Deviation Range	2% Parameter Deviation Range
P1 (E Model)	**B_x Life at 1%**	5.6775E+30	4.1836E+30
	B_x Life at 10%	6.4548E+30	5.4326E+30
	B_x Life at 50%	7.5539E+30	7.4733E+30
P2 (1/E Model)	**B_x Life at 1%**	7.0942E+28	5.2218E+28
	B_x Life at 10%	8.0776E+28	6.8087E+28
	B_x Life at 50%	9.4618E+28	9.3790E+28
P3 (E Model)	**B_x Life at 1%**	5.0578E+29	3.7374E+29
	B_x Life at 10%	5.7601E+29	4.8594E+29
	B_x Life at 50%	6.7425E+29	6.6871E+29

Table 14: Results of HCI for N-channel and P-channel as B_x Life.

HCI B_x Life Estimates for P1, P2, and P3		1% Parameter Deviation Range	2% Parameter Deviation Range
N-channel			
P1	**B_x Life at 1%**	4.5386E+22	4.4991E+22

HCI B_x Life Estimates for P1, P2, and P3		1% Parameter Deviation Range	2% Parameter Deviation Range
	B_x Life at 10%	5.2653E+22	5.2411E+22
	B_x Life at 50%	6.3161E+22	6.3155E+22
P2	**B_x Life at 1%**	0.7881E+20	0.7796E+20
	B_x Life at 10%	0.8937E+20	0.8886E+20
	B_x Life at 50%	1.0433E+20	1.0431E+20
P3	**B_x Life at 1%**	3.7694E+20	3.7325E+20
	B_x Life at 10%	4.3015E+20	42778E+20
	B_x Life at 50%	5.0551E+20	5.0555E+20
P-channel			
P1 (L > 0.25 µm)	**B_x Life at 1%**	4.3372E+15	4.3307E+15
	B_x Life at 10%	5.0378E+15	5.0266E+15
	B_x Life at 50%	6.0439E+15	6.0327E+15
P2 (L < 0.25 µm)	**B_x Life at 1%**	1.3104E+19	1.3301E+19
	B_x Life at 10%	1.4859E+19	1.4795E+19
	B_x Life at 50%	1.7331E+19	1.7330E+19
P3 (L < 0.25 µm)	**B_x Life at 1%**	6.2689E+19	6.2169E+19
	B_x Life at 10%	7.1469E+19	7.1136E+19
	B_x Life at 50%	8.3951E+19	8.3873E+19

From the obtained results, one can rank the parts concerning the failure mechanism of interest and select the best of all or a few parts as per the ranking. The ranking of the parts is

shown in Table 15. Further, the deviation of just 1% additional has created a significant change in the estimated TTF values EM and TDDB, but for the HCI, the values are similar. If the scale factor is known, one can even identify the accurate TTF values of a part from this approach which is currently limited to ranking as these values are not scaled using the scale factor. Based on the results, the best part for EM is P1, for TDDB is P2, for HCI N-channel, it is P1, and for P-channel, it is P2.

Table 15: Ranking of the parts based on B_x life results obtained through MATLAB GUI.

Rank	**Ranking of the Parts P1, P2, and P3**			
	EM	**TDDB**	**HCI (N-channel)**	**HCI (P-channel)**
1	P1	P1	P1	P3
2	P2	P3	P3	P2
3	P3	P2	P2	P1

6. Summary of Approach, Contributions, and Future Work

When they do, electronic part manufacturers provide reliability information in terms of the MTBF or FIT rates, both with underlying constant failure rate assumptions. However, a constant failure rate (which assumes an exponential time to failure distribution) as a reliability metric value does not account for the damage accumulation. Furthermore, the constant failure rate as a reliability metric is based on the assumptions that the failures during operation are random and that there is no wear-out, two rarely true assumptions for electronics. The approach demonstrated in this work provides a concrete methodology to assist users in assessing active electronic parts' reliability by estimating time to failure for die-level failure mechanisms based on factors such as part architecture, materials, reliability requirements, and life cycle profile. It further utilizes the estimated time to failure (TTF) distributions of the parts to assist in part selection-related decisions.

6.1. Approach and Contributions

This thesis makes significant contributions to the field of part selection by focusing on estimated time-to-failure (TTF) values for critical die-level failure mechanisms. The first contribution lies in the comprehensive idea of how part manufacturers avoid sharing critical information with the users or customers, which hinders the complete understanding of the part and the part selection-related decision-making. The project focuses on four key failure mechanisms: electromigration (EM), time-dependent dielectric breakdown (TDDB), hot carrier injection (HCI), and negative bias temperature instability (NBTI). The thesis establishes a strong foundation for understanding their impact on part selection and overall reliability by recognizing and emphasizing these mechanisms.

An extensive literature review is conducted to ensure a comprehensive understanding of the failure mechanisms. This review delves into the details of each mechanism, encompassing their associated failure models that can predict TTF values. The thesis focuses explicitly on the models provided in the JEP122 standard, developed based on a thorough analysis of literature and industry response. This reliance on established industry standards ensures a robust framework for estimating TTF values.

A crucial aspect of part selection is the consideration of process technology and the geometric features of the part. The thesis presents a methodology to obtain process technology information from part-related documents. This methodology enables the selection of appropriate failure models based on the specific parameters associated with the part's geometric characteristics.

In order to estimate TTF values, it is necessary to identify the parameters required by the selected failure models. The thesis outlines the parameter identification process, drawing information from various sources. It is important to note that the parameters are considered distributions rather than constant values due to the approximate nature of experimental information. TTF distributions are obtained and represented as histograms by plugging these parameter ranges into the models.

The obtained TTF distributions are further converted into cumulative distribution function (CDF) plots. These plots enable the ranking of failure mechanisms and facilitate part selection based on desired reliability requirements. By adjusting the application conditions, suitable parts can be identified to meet specific user requirements, providing a practical and customizable approach to part selection. The MATLAB GUI creates a user-friendly platform to identify the best parts or rank the parts based on the required application conditions.

This thesis makes notable contributions by offering a systematic approach to part selection based on estimated TTF values for critical die-level failure mechanisms. Through a comprehensive literature review, process technology identification, parameter estimation, and ranking techniques, the thesis provides valuable insights for informed decision-making in part selection, ultimately leading to enhanced reliability in integrated circuits.

6.2. Future Work

In the context of the thesis, several avenues for future work can be explored to advance the field of part selection based on estimated TTF values for die-level failure mechanisms. Firstly, developing a process or methodology to store the part-specific information as a database that can be accessed in the future to understand the changes in failure mechanisms, parameter trends, and many more.

Enhancing the accuracy of parameter estimation is another area for future research. Employing advanced statistical techniques or machine learning algorithms to refine the distribution estimation of parameters would reduce approximation errors and lead to more precise predictions of TTF values. This improved parameter estimation would contribute to the reliability assessment and selection of parts.

Integrating advanced reliability models that extend beyond the JEP122 standard would be a valuable direction for future work. By incorporating alternative models or combining multiple models, a more comprehensive and refined estimation of TTF values can be achieved, enhancing the reliability analysis and providing more accurate predictions.

Expanding the scope of the thesis by considering additional failure mechanisms beyond EM, TDDB, HCI, and NBTI presents an exciting opportunity for future work. Incorporating other

relevant failure mechanisms would result in a more comprehensive part selection process, enabling a broader assessment of reliability concerns and improving the overall effectiveness of part selection.

Identifying the scale factor value for each process technology can provide accurate TTF values rather than the scaled TTF results shown in this work. Accurate TTF values can create a massive breakthrough as one can identify the part TTF considering multiple failure mechanisms. We selected parts for a failure mechanism in the methodology used to perform the part selection. In Figure 44, the methodology helps to identify the parts TTF considering all the failure mechanisms of interest. Since we know the exact TTF values, we can compare the TTF values obtained for all failure mechanisms of a part and pick the least TTF result as the TTF because the part requires one failure due to a mechanism to be considered a failed part. Performing this process helps identify the TTF of all n different parts, which can be ranked based on B_x life as in our previous methodology.

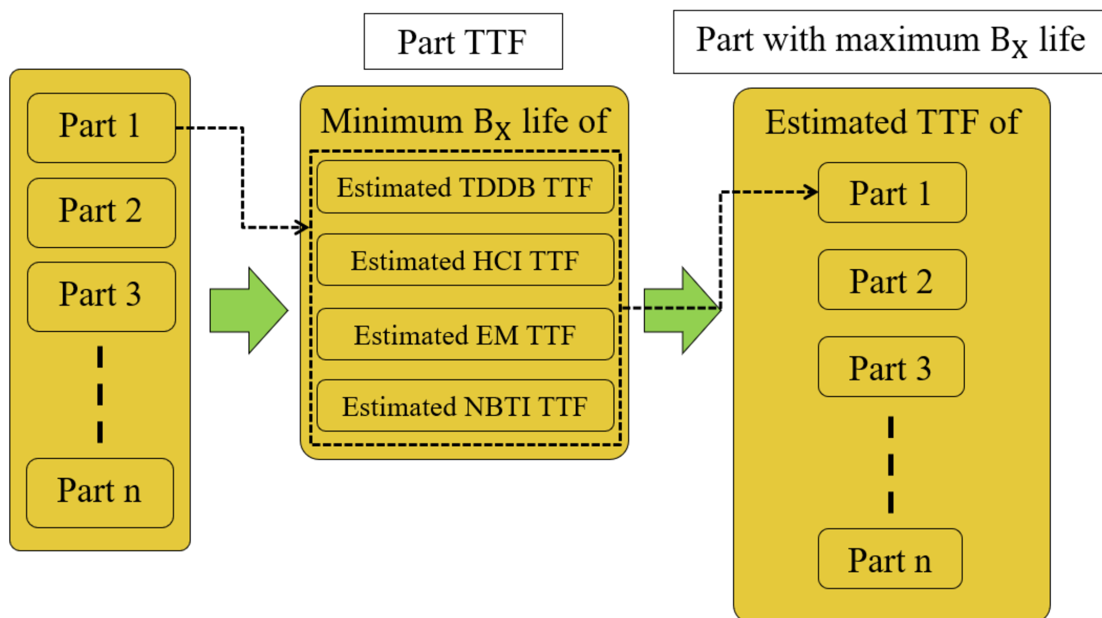


Figure 44: Part selection methodology considering multiple failure mechanisms.

Addressing these areas for future work would contribute to the refinement, applicability, and customization of the part selection process based on estimated TTF values. These advancements would improve reliability and performance in integrated circuits, enhancing the overall quality and effectiveness of part selection methodologies.

Appendices

Appendix A: Time to Failure Distribution MATLAB Script of EM

```
clc

clear

A = normrnd(Mean, Standard Deviation, 1000); %Scale parameter (Time Units)

T = normrnd(Mean, Standard Deviation, 1000); %User defined temperature (K)

Eaa = normrnd(Mean, Standard Deviation, 1000); %Activation Energy (eV)

Area = normrnd(Mean, Standard Deviation, 1000); %Interconnect Area (μm^2)

I = normrnd(Mean, Standard Deviation, 1000); %Current (mA)

J = I./Area;

n = normrnd(Mean, Standard Deviation, 1000); %Model Constant Exponent

TTF = A.*((J).^(-n)).*exp(Eaa./((8.62*10^-5).*T)); %Time to Failure Calculation

h = histogram(TTF,100,'Normalization','cdf');

xlabel("TTF")

ylabel("CDF")

Values = h.Values;

BinCenters = (h.BinEdges(1:end-1)+h.BinEdges(2:end))/2;

% Eliminate any flat parts of the CDF:

FlatValues = find(diff([h.Values])==0)+1;
```

```
Values(FlatValues) = [];

BinCenters(FlatValues) = [];

percentiles = interp1(Values,BinCenters,[Bx%]) %Plug in x value in percent
```

Appendix B: Time to Failure Distribution MATLAB Script of TDDB E Model

```
clc

clear

A = normrnd(Mean, Standard Deviation, 1000); %Scale parameter (Time Units)

T = normrnd(Mean, Standard Deviation, 1000); %User defined temperature (K)

Eaa = normrnd(Mean, Standard Deviation, 1000); %Activation Energy (eV)

Y = normrnd(Mean, Standard Deviation, 1000); %Field Acceleration (cm/MV)

Vg = normrnd(Mean, Standard Deviation, 1000); %Gate Voltage (V)

to = normrnd(Mean, Standard Deviation, 1000); %Gate Oxide Thickness (nm)

Eox = Vg./ to;

TTF = A.*exp(-Y.*Eox).*exp(Eaa./((8.62*10^-5).*T)); %Time to Failure Calculation

h = histogram(TTF,100,'Normalization','cdf');

xlabel("TTF")

ylabel("CDF")

Values = h.Values;
```

```
BinCenters = (h.BinEdges(1:end-1)+h.BinEdges(2:end))/2;

% Eliminate any flat parts of the CDF:

FlatValues = find(diff([h.Values])==0)+1;

Values(FlatValues) = [];

BinCenters(FlatValues) = [];

percentiles = interp1(Values,BinCenters,[ Bx%]) %Plug in x value in percent
```

Appendix C: Time to Failure Distribution MATLAB Script of TDDB 1/E Model

```
clc

clear

T = normrnd(Mean, Standard Deviation, 1000); %Scale Parameter (Time Units)

G = normrnd(Mean, Standard Deviation, 1000); %Field Acceleration (MV/cm)

Vg = normrnd(Mean, Standard Deviation, 1000); %Gate Voltage (V)

to = normrnd(Mean, Standard Deviation, 1000); %Gate Oxide Thickness (nm)

TTF = T.*exp(G.*(to./ Vg)); %Time to Failure Calculation

h = histogram(TTF,100,'Normalization','cdf');

xlabel("TTF")

ylabel("CDF")

Values = h.Values;
```

```
BinCenters = (h.BinEdges(1:end-1)+h.BinEdges(2:end))/2;

% Eliminate any flat parts of the CDF:

FlatValues = find(diff([h.Values])==0)+1;

Values(FlatValues) = [];

BinCenters(FlatValues) = [];

percentiles = interp1(Values,BinCenters,[Bx%]) %Plug in x value in percent
```

Appendix D: Time to Failure Distribution MATLAB Script of HCI Model

```
clc

clear

A = normrnd(Mean, Standard Deviation, 1000); %Scale parameter (Time Units)

T = normrnd(Mean, Standard Deviation, 1000); %User defined temperature (K)

n = normrnd(Mean, Standard Deviation, 1000); %Exponent

Eaa = normrnd(Mean, Standard Deviation, 1000); % Activation Energy (eV)

I = normrnd(Mean, Standard Deviation, 1000); %Current (mA)

L = normrnd(Mean, Standard Deviation, 1000);%Channel length (µm)

TTF = A.*((I./L).^(-n)).*exp(Eaa./((8.62*10^-5).*T)); %Time to Failure Calculation

h = histogram(TTF,100,'Normalization','cdf');

xlabel("TTF")

ylabel("CDF")
```

```
Values = h.Values;

BinCenters = (h.BinEdges(1:end-1)+h.BinEdges(2:end))/2;

% Eliminate any flat parts of the CDF:

FlatValues = find(diff([h.Values])==0)+1;

Values(FlatValues) = [];

BinCenters(FlatValues) = [];

percentiles = interp1(Values,BinCenters,[Bx%]) %Plug in x value in percent
```

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