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A Computer Aided Engineering Program for Coplanar and In-Line Printed Wiring Board Thermal and Thermal Reliability Analysis

by

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SUMMARY

This report is a review of the cooperative: Westinghouse - University of Maryland, Mechanical Engineering, computer-aided-design (CAD) of a printed wiring board (PWB) project. In earlier cooperation (1984) with Westinghouse, an interface link was developed between the computer-aided PWB layout and routing routine (RECAL-REDAC) and a thermal analysis routine. A CAD program, called MTEMP resulted, which performs a thermal analysis for in-line PWBs without the requirements of "hand" scaling and node shifting used by previous programs, eliminates much of the I/O by providing a direct link with REDAC, and provides an accurate graphical model of the PWB. Finally, to control development cost and conform to copywrites, MTEMP does not alter REDAC.

Our research effort over the 1985 year consisted of developing a coplanar thermal analysis program and a thermal reliability analysis program which was integrated into a user friendly printed wiring board design program. In addition heat dissipation input for each component can now be manually entered or can be accessed from the working database. A component database shell was developed that will aid in the thermal and reliability analysis and can be called from any routine as needed. This solves one of the past limitations in that there was no reference from the PWB components to the actual part numbers.

ACCOMPLISHMENTS

- Flow of information between the RACAL-REDAC software used by Westinghouse and the PWB design programs was established. A program was developed whereby REDAC files from a VAX could be directly downloaded and translated for use by an IBM-PC.

- Set up a global data base which includes typical and maximum component heat dissipation values and the Military Standards 217-D for digital micro-electronic components.

- Set up a working database which contains information for the specific PWB under design. This includes component dimensions and orientation, board dimensions, thermal and reliability data and identifiers.

- Developed thermal analysis programs for coplanar PWBs.

- Developed a thermal reliability program to calculate component and board reliabilities using typical and maximium power values in conformance with MIL-STD 217-D requirements.

- Developed a graphic interface to display thermal and reliability information.

- Linked the reliability program to the thermal analysis program.

- Linked the reliability program to the MIL-STD 217-D global data base.

DATA BASE INFORMATION

MTEMP reads three files that REDAC generates. The file BOA contains the PWB outline. The file LIB contains the rectangular outline coordinates of the components used in the design, as well as the pad locations. The third file, COM, contains the components used on a particular board and their location and orientation on the board. Each component for a particular PWB is read from the COM file. Then the corresponding component is located from the LIB file. The lower left hand pad is calculated and the component is rotated accordingly. The rectangular outline of the component is plotted on the display screen. The components are also labeled with the component identifier, from the COM file, on the display screen and the centers of each component are marked for rail placement.

Data base management was a key issue in the 1985 project. In general, the transfer from one functional operation to another requires the intermediate steps of data conversion, data transfer and decision making by an expert engineer. A global database (COMPDATA) has been developed to hold thermal reliability data (to be discussed in the section on Thermal Reliability), and typical and maximium heat dissipation values. The working database is developed to hold this information also, but only for the PWB which is presently being designed. In addition, the working database holds all the component identifiers, junction and case temperatures, cooling parameters and board parameters for the PWB under design.

THERMAL ANALYSIS OF A PRINTED CIRCUIT BOARD

In-Line PWBs : One function of MTEMP is in the design of conductance strips or rails. By determining adjacent components and using production rules, the horizontal rails passing through the center of the components are calculated and graphically displayed. Adjacent components are established in a file for the conductance routine. Once horizontal adjacent components have been determined, the edge components are calculated along with the vertical conductance along the edge. A thermal finite difference routine is then employed to solve the steady-state conductance problem. An equation is formulated for each node and the set of equations solved for the temperatures throughout the board.

$$q_i + \sum_j \frac{(T_j - T_i)}{R_{ij}} = 0$$

where R_{ij} is the thermal resistance. The temperatures are then plotted on the screen along with the rails and component numbers. The user has the option of changing some input information such as size of rails and heat sink temperatures. Program execution time for very dense boards is approximately 3 minutes when run on a IBM PC.

Coplanar PWBs : This program was translated into BASIC to run on the IBM-PC. The fundamental program was taken from one used by Westinghouse, but was modified for direct input from the working database, for via a manual input of heat dissipation values. Flow rows can now be placed in an interactive mode. Calculation time for a two sided PWB with 100 components per side and standard fin structures is about 10 minutes in compiled mode. All the graphics routines are linked to this analysis so that the component junction temperature, case

temperature, and the air temperature can be displayed. In addition, a tabular form of the data can be presented for analysis.

THERMAL RELIABILITY

Thermal reliability analysis requires a thermal analysis of the PWB with knowledge of the cooling technology, the global package technology (board, composition, and configuration), the local package and interconnection technology, the microcomponent technology (SSI, MSI, LSI, VLSI) and the component circuit family (TTL, ECL, MOS etc.). This data resides in the working data base. Component reliability is measured as the number of failures per million hours of operation, while the total board failure rate is the sum of the component failure rates.

The component types we are considering are listed in MIL-STD 217-D as Monolithic Microelectronic Devices. The equations for calculating reliability are listed on pages 5.1.2-1 through 5.1.2.4. There are five basic categories:

1.) Bipolar & MOS Digital (Small/Medium scale integration)
2.) Bipolar & MOS Linear
3.) Bipolar & MOS Random Logic (Large scale integration)
4.) Random Access Memories (RAM)
5.) Read only Memories (ROM and PROM)

The calculation for reliability λ_ρ for these components is:

$$\lambda_\rho = \pi_Q * \{C_1 * \pi_T * \pi_V * \pi_{PT}) + (C_2 + C_3) * \pi_E\} * \pi_L$$

where

λ_ρ = Device failure rate per million hours

π_Q = Device quality factor

π_T = Temperature acceleration factor

π_V = Voltage derating stress factor

π_E = Application environment factor

C_1 & C_2 = Circuit complexity factors

C_3 = Package complexity factor

π_L = Device learning factor

π_{PT} = PROM programming technique factor.

The quality factor π_Q is based on the procurement standard used when purchasing the part, and ranges from .5 to 35. The highest quality parts meet the requirements for MIL-M-38510, and for these parts π_Q is .5. The range extends all the way down to parts purchased commercially "off-the shelf" and have a quality factor of 35. Note that as part quality goes down, reliability increases as evidenced by the equation. Descriptions of device quality and the associated numerical values are in MIL-STD 217, pp. 5.1.2.5-1 - 5.1.2.5-2.

The temperature acceleration factor π_T may be determined in two ways. An equation exists for calculating π_T on pp. 5.1.2.5-4 of the MIL-STD. This equation is:

$$\pi_T = 0.1 * EXP(x)$$

where

$$x = -A * (1/ (T + 273) - 1/298)$$

A = Tabulated value base on component type

T = Component junction temperature

Alternatively, empirically determined values for π_T are tabulated in tables 5.1.2.5-5 - 5.1.2.5-13. For programming purposes, π_T is found using the above equation. If the temperature is ambient at 25°C, π_T = 1.0. Note that as temperature increases, π_T increases as the negative exponent becomes smaller, resulting in higher failure rate. For a hermetically sealed CMOS component at 50°C, π_T = 0.71. This is a 700% increase, and though the numbers are small the change is significant.

The voltage derating stress factor π_V is basically the same for all component types and generally has a value of 1.0. The only exception is for CMOS components with a supply voltage in excess of 5 volts. In this case, the military standard supplies two equations for the calculation of π_V. These equations are used if the supply voltage (VDD) is between 12 and 20 volts. The general form of the equation is:

$$\pi_V = A * EXP(X)$$

where

$$X = \{ B * V_{DD} * (T + 273) \} / 298$$

For 12 < V_{DD} < 15.5 volts, A = 0.110 and B = 0.168. For 18 < V_{DD} < 20 volts, A = 0.68 and B = 0.135. For V_{DD} - 12 volts operating at a temperature of 30°C, π_V is 0.854. On the other extreme, for a supply voltage of 20 volts and an operating temperature of 50°, π_V = 1.27. This factor does not carry nearly the same impact as the quality.

The application environment factor π_E is based on the conditions under which the part will be used. An extnesive listing of various operational conditions is given in the MIL-STD in table 5.1.1-3. The corresponding numerical values for these different environments are given in table 5.1.2.5-3. π_E ranges from 0.38 for a non-mobile laboratory environment to 220 if the part must experience a cannon launch. This is an extremely high number; typical values of π_E vary from 0.38 to about 13. The environmental factor is therefore on a similar order with the quality factor.

The circuit complexity factors C_1 and C_2 vary more with component type than do the others. They are strong functions of the number of bits or gates on the component. The coefficients vary, but the general form is:

$$C = AC * (N)^{B}$$

where

A	= Tabulated valued based on component type
B	= Tabulated exponent based on component type
N	= Number of bits or gates

An increase in the number of bits or gates on a component dramatically affects C_1 and C_2 since failures related to circuit complexity vary as that number raised to a power. Values for A and B are given in the MIL-STD 217D in tables 5.1.2.5-17 - 5.1.2.5-24.

The package complexity factor C_3 is calculated with a formula of the same type as that used for C_1 and C_2. Values for A and B are given in the MIL-STD 217D in table 5.1.2.5-26.

The learning factor π_L is incorporated to accomodate changes in design of components over time. The value of π_L is taken to be 1 unless the component is in initial production or major changes in design have occurred, in which case it is taken to be 10.

The factor π_{PT} is for PROM's and takes into consideration the method used to program the PROM. Π_{PT} is taken to be 1.0 with the exception of two cases. In the first case, if the PROM is Bipolar and the programming technique was N_iC_r, T_iW Polysilicon links, or Shorted Junction, then:

$$\pi_{PT} = 0.985 + 9.5 * 10^{-5} (B)$$

where B = number of bits. In the second case, if the PROM is both a MOS device and an EPROM, then:

$$\pi_{PT} = 0.950 + 7.5 * 10^{-5} (B)$$

where B is again the number of bits. Note that with the exception of only a few cases π_{PT} is always 1.0, and even for the special cases it is very close to 1.0.

Section 5.2 of MIL-STD 217 gives a method of calculating the total board failure rates based on the failure rates of the components. It is denoted λ_t, and can be found as the sum of the individual component failure rates with a quality factor attached. Thus the total board failure rate is:

$$\lambda_t = \sum_{i=1}^{n} N_i (\lambda_g * \pi_Q)_i$$

where

λ_t = Total equipment failure rate

λ_g = Generic failure rate for the ith generic part

π_Q = Quality factor for the ith part

N_i = Quality of the ith part

n = Number of different generic part numbers

The values for π_Q are tabulated in section 5.1 as previously described. The MIL-STD lists generic failure rates λ_g for different component types under various operating conditions, tabulated in tables 5.2-1 - 5.2-22. When these values are used it is necessary to multiply in the quality factor. However, if the methods of section 5.1 are used, the quality factor is already included, and then the total board failure rate is simply the sum of the component failure rates calculated using the equation for λ_t.

The program RELSUB calculates thermal reliability for components based on their characteristics and temperature, following the MIL-STD 217-D. In order to perform this reliability analysis, certain parameters must be known: component part number, number of bits or gates on the component, number of pins on the component, and component type (TTL vs. MOS, Digital vs. Linear vs. PROM vs. RAM). This data is in the working database.

GRAPHICS

The graphics package runs on data generated by other subroutines which provide location, component size, component identity and some analysis attributes such as temperature, or reliability. The graphics program is presently used to

- draw the PWB board, components and component information
- color code component temperatures
- color code component reliability

The program stores pictures and temperature data to print the temperature on each component. The total temperature range is divided into thirds and the components colored from coolest to hottest as green, yellow and red. This provision is made only because we are currently limited to three colors by the software. Another provision is a temperature and reliability color legend window which toggles on and off when viewing the respective color plot. All color plots are saved and may be recalled later.

DISCUSSION OF ARTIFICIAL INTELLIGENCE TECHNIQUES

The increased demand for high performance electronic circuits has necessitated the need for more sophisticated and rigid design specifications and has thus necessitated the utilization of computer-aided engineering design (CAD) and artificial intelligence (AI) techniques. Presently, the range of design operations which can be effectively handles using CAD include: component placement based on geometric constraints, rouiting analysis, thermal analysis, design and tolerance checks, the generation of manufacturing data and computer numerical control tapes, and documentation [3,4,5,6]. However, increased complexity in electronic packaging will require checks on reliability as well. Advanced computer-aided engineering and AI in the form of decision support, adaptive learning, and knowledge based engineering will be important.

As an example, with other factors fixed, the cooling technology determines the component and board temperatures which are computed by a thermal computational routine. These temperatures directly result in a thermal reliability estimate through MIL-STD 217D specifications. Component rearrangement at this stage thus requires decision support based on a knowledge base to anticipate how the geometric constraints introduced by the mode of cooling i.e. conduction or forced air cooled, can be accomodated. On the larger scale, factors such as interconnection wire length and the number of board laryers for wire routing must also be considered. In this case, an embedded expert system would require that decision on the functional level (component rearrangement) be subject to decisions on the global level (the interaction between design goals).

PUBLICATIONS

"Computer-Aided Heat Sink Design for Printed Wiring Boards", M. Pecht, M. Palmer and J. Horan, accepted for presentation and publication: ICCAD-85, November 18-22, 1985.

"Intelligent Design of Printed Wiring Boards", J. Horan, M. Palmer, M. Pecht and Y. Wong, Proceedings: Association for Computing Machinery, Vol.1, pp.123, (1985).

GRANTS WHICH SUPPLEMENT THE WESTINGHOUSE EFFORT

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